

MS-7A39 Ver:1.0

CPU:
AMD AM4

System Chipset:
Promontory A320
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

VRM
RT8894 3+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H

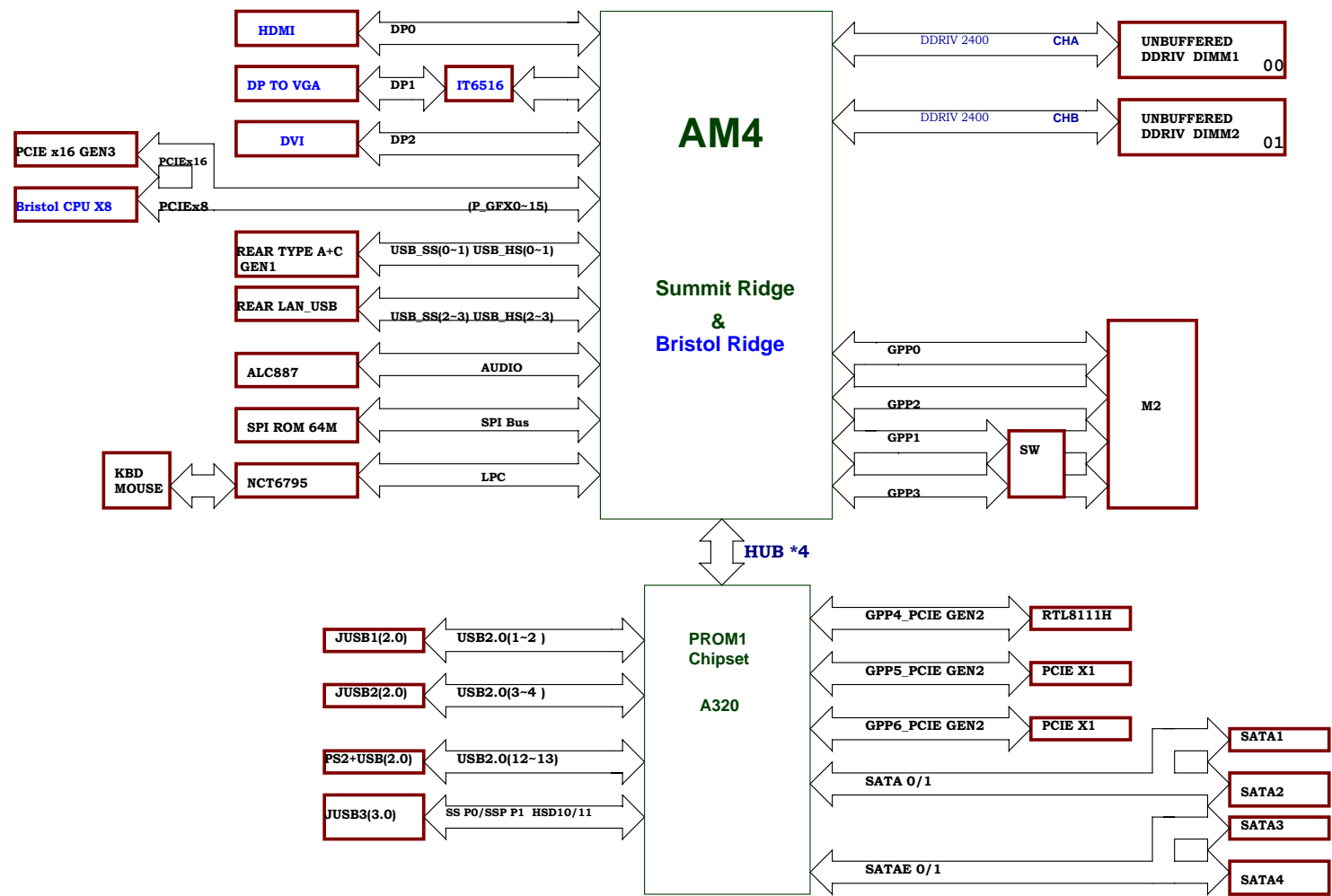
Azalia CODEC - Realtek
ALC887

Expansion Slots:

From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

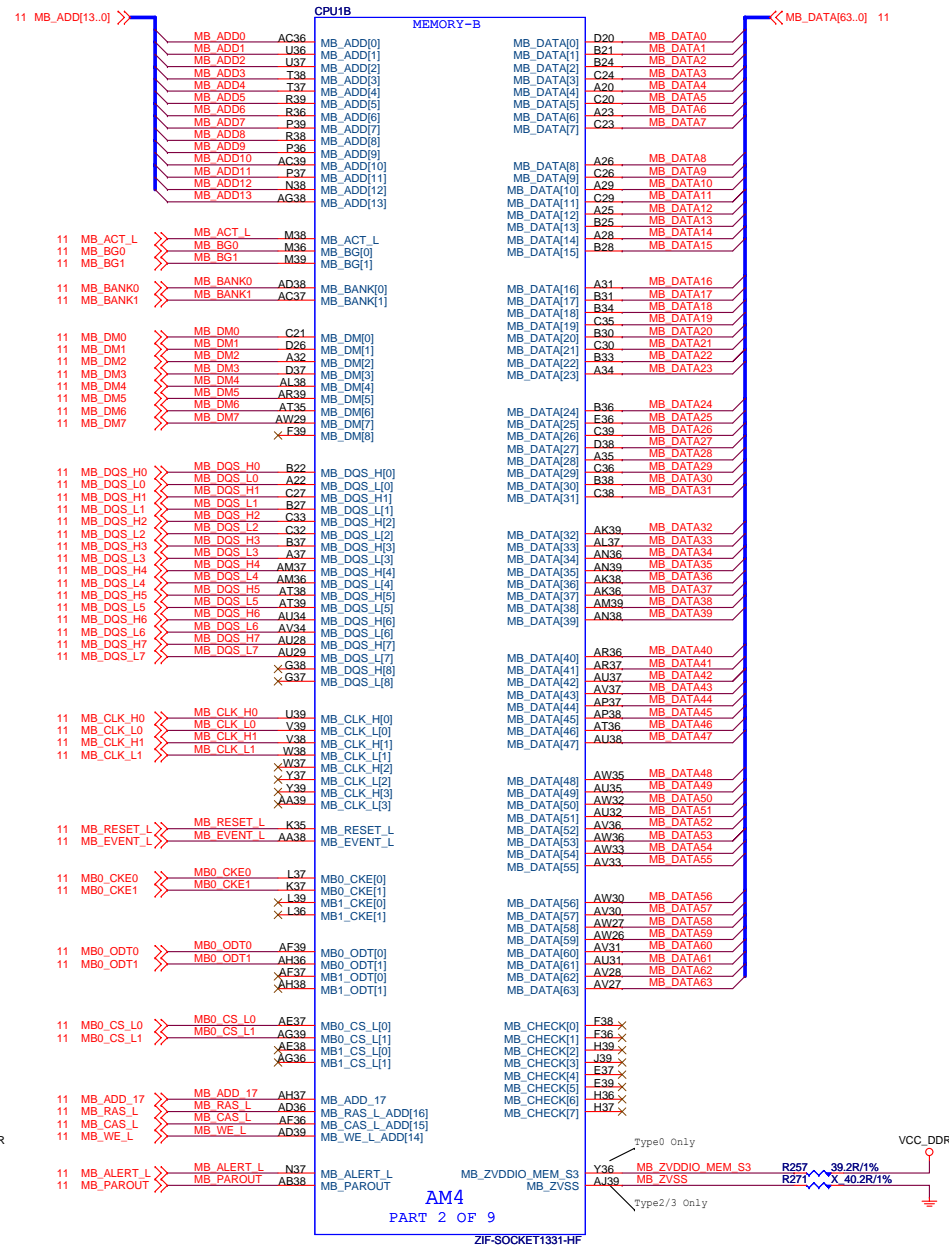
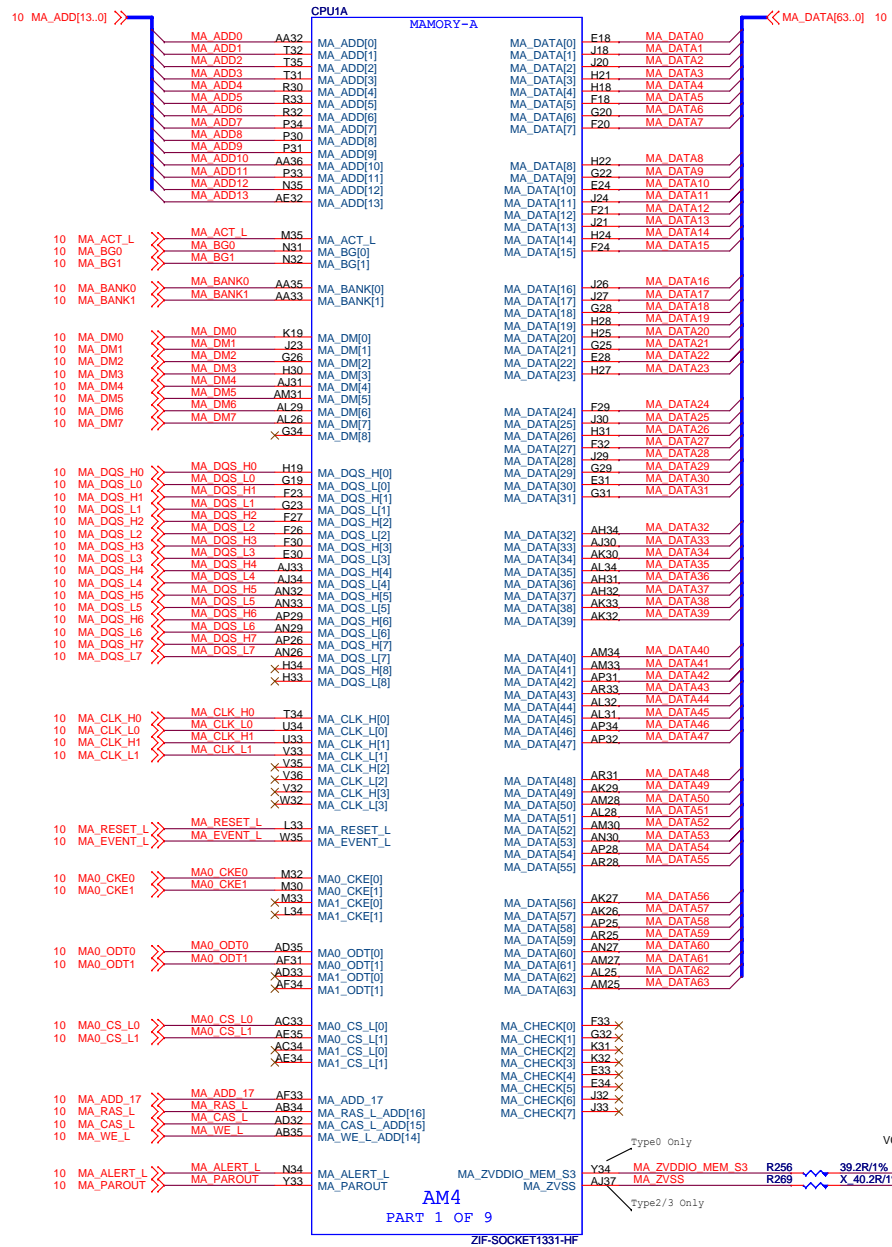
OCP IC:
UP6273

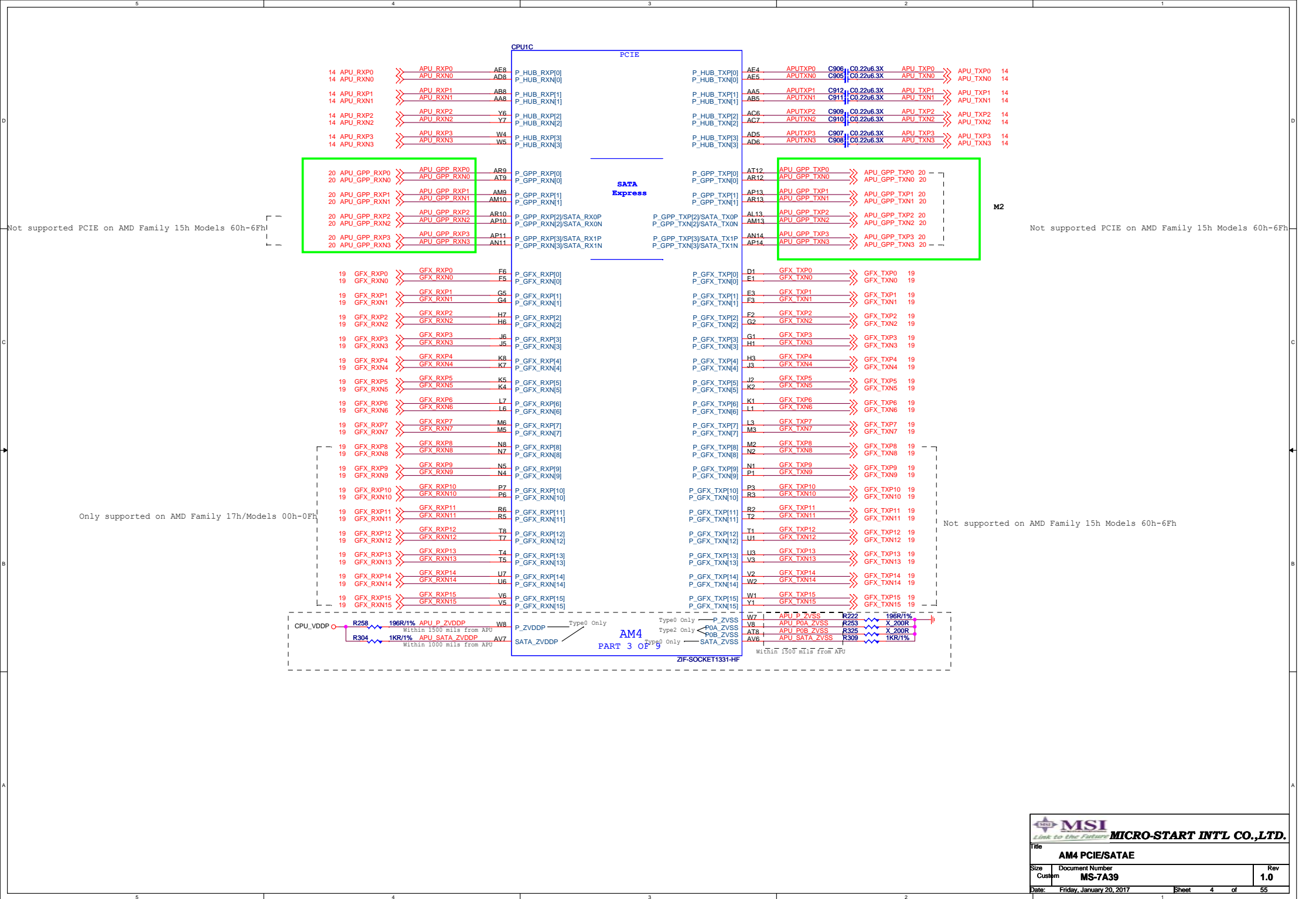
FUSION BLOCK DIAGRAM

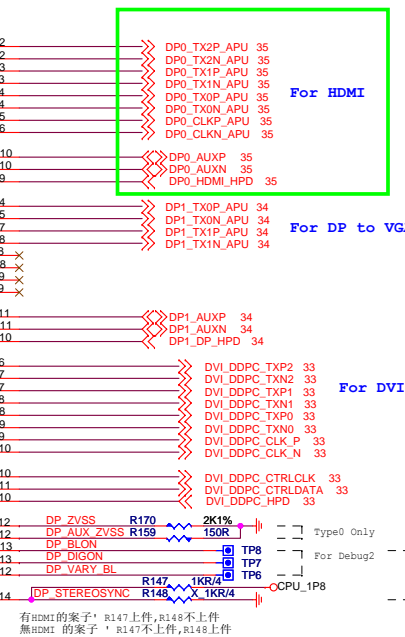


AMD AM4

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29 DVI Connector	
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31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTM-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	



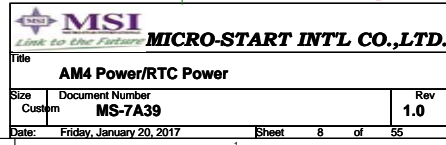


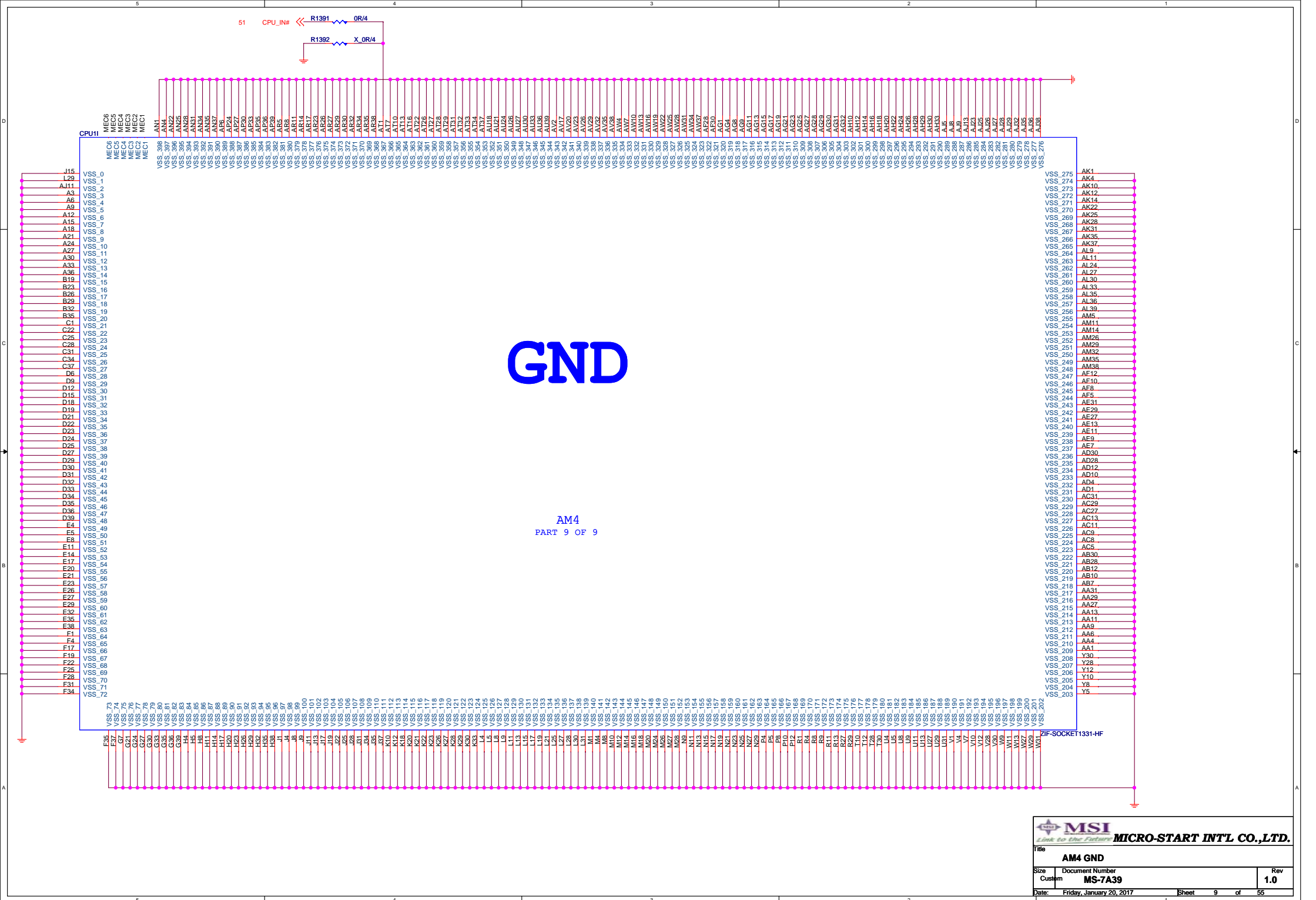


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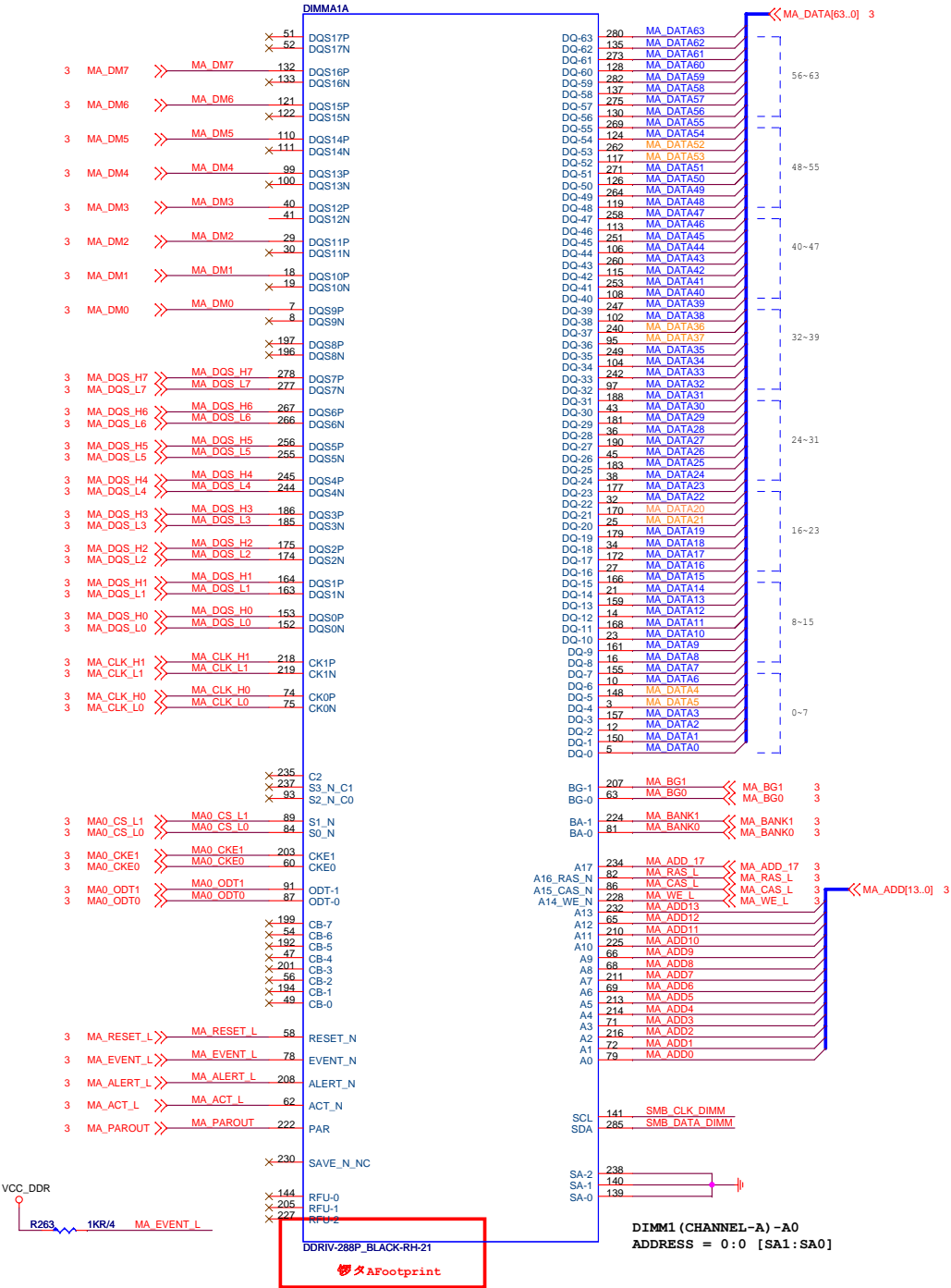
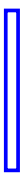
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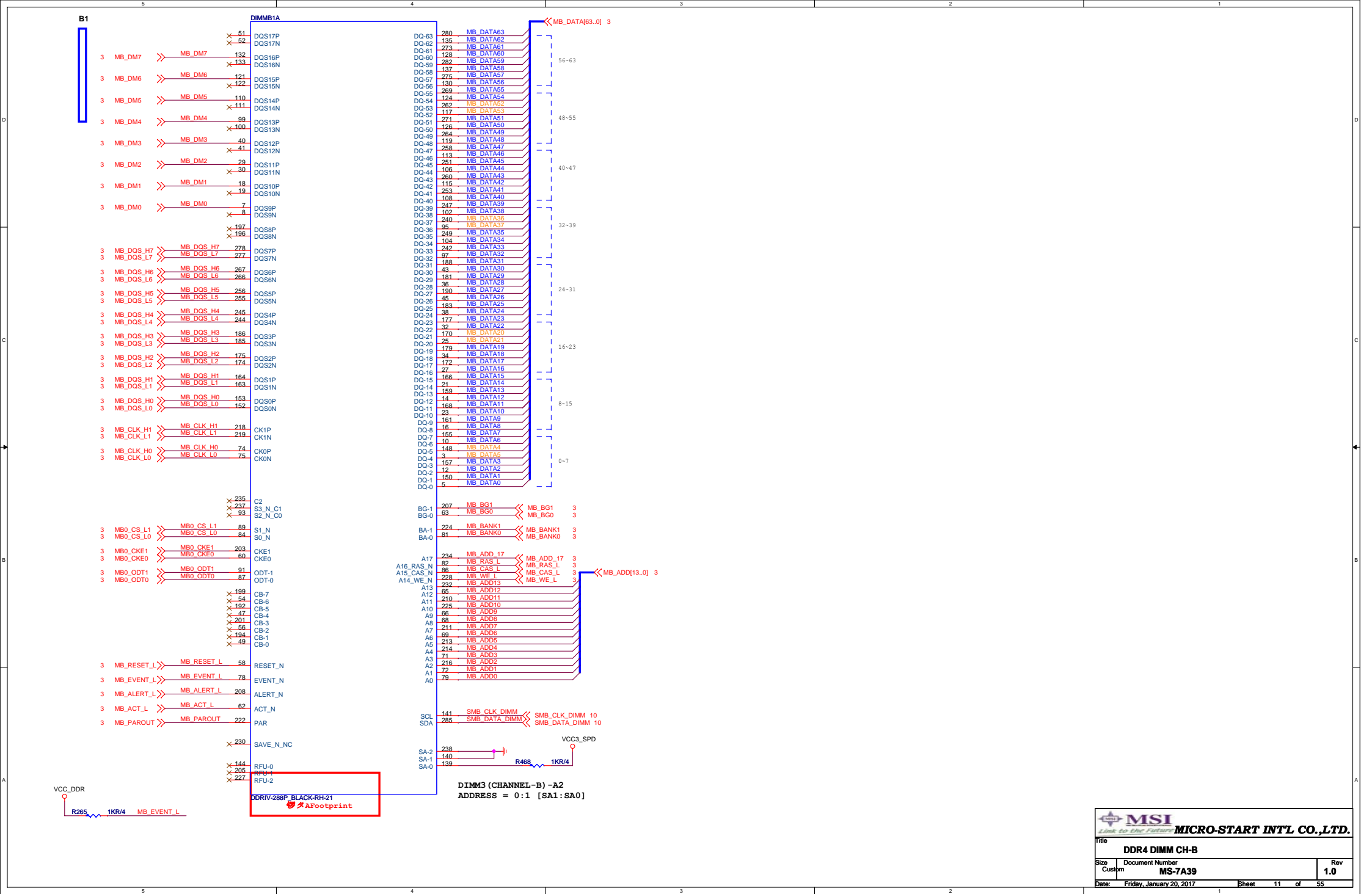



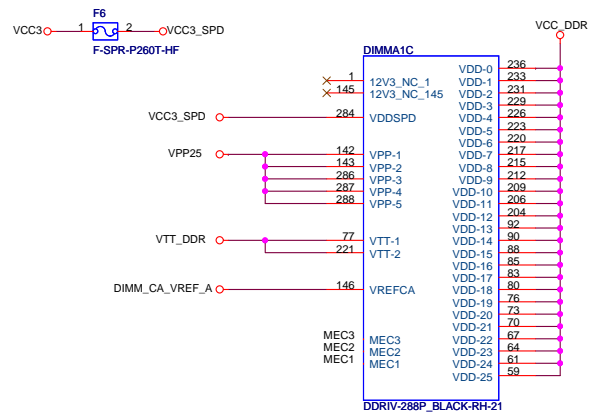


A1

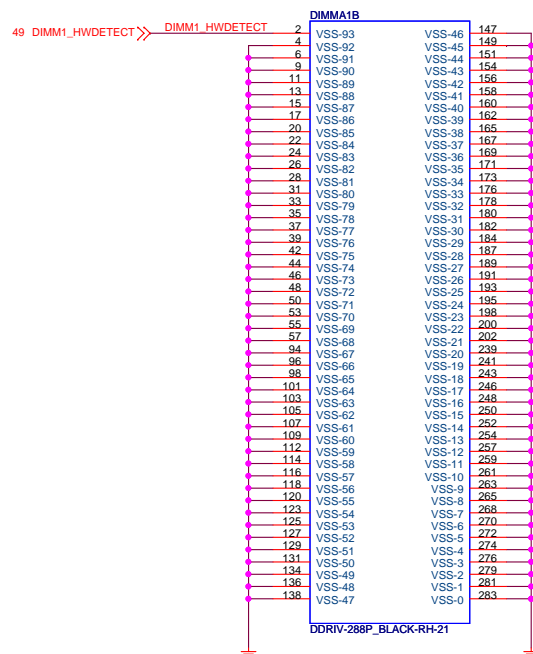
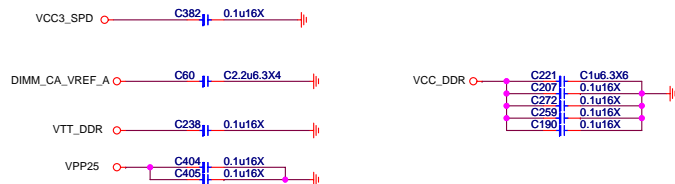


6.43.46.51 SCLK0 >> SCLK0 R427 OR/4 SMB_CLK_DIMM >> SMB_CLK_DIMM 11
6.43.46.51 SDATA0 >> SDATA0 R431 OR/4 SMB_DATA_DIMM >> SMB_DATA_DIMM 11



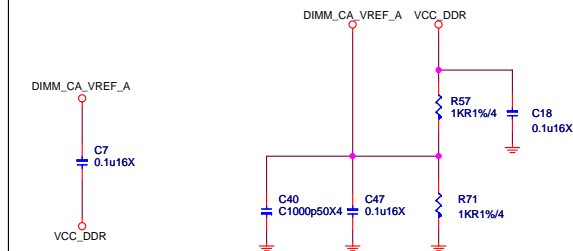


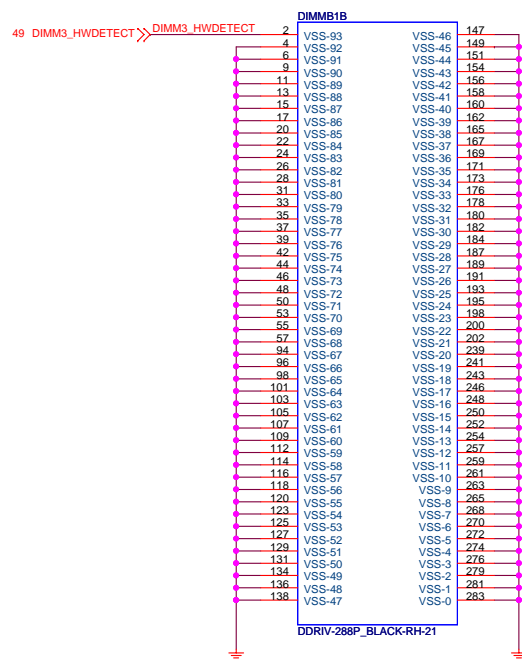
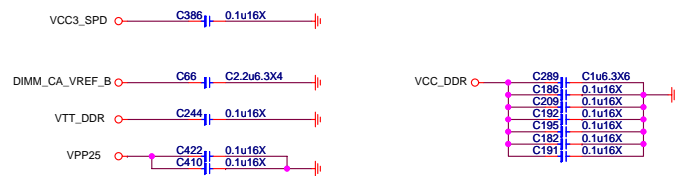
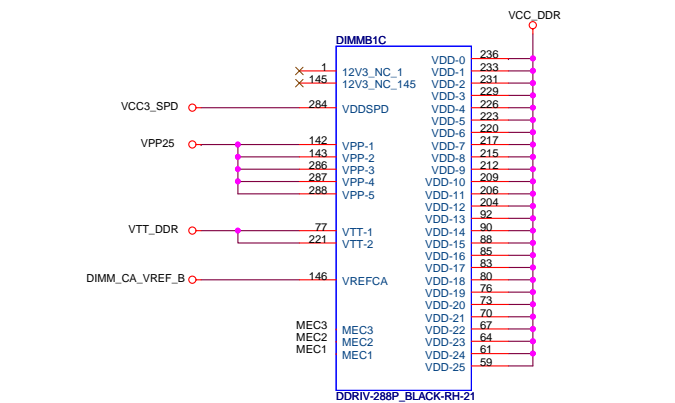
DIMM SLOT PN BY SPEC



DDR VREF

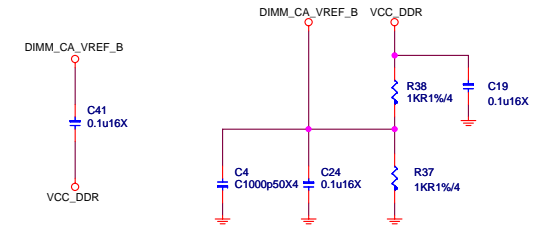
(place resistors close to DIMMs)

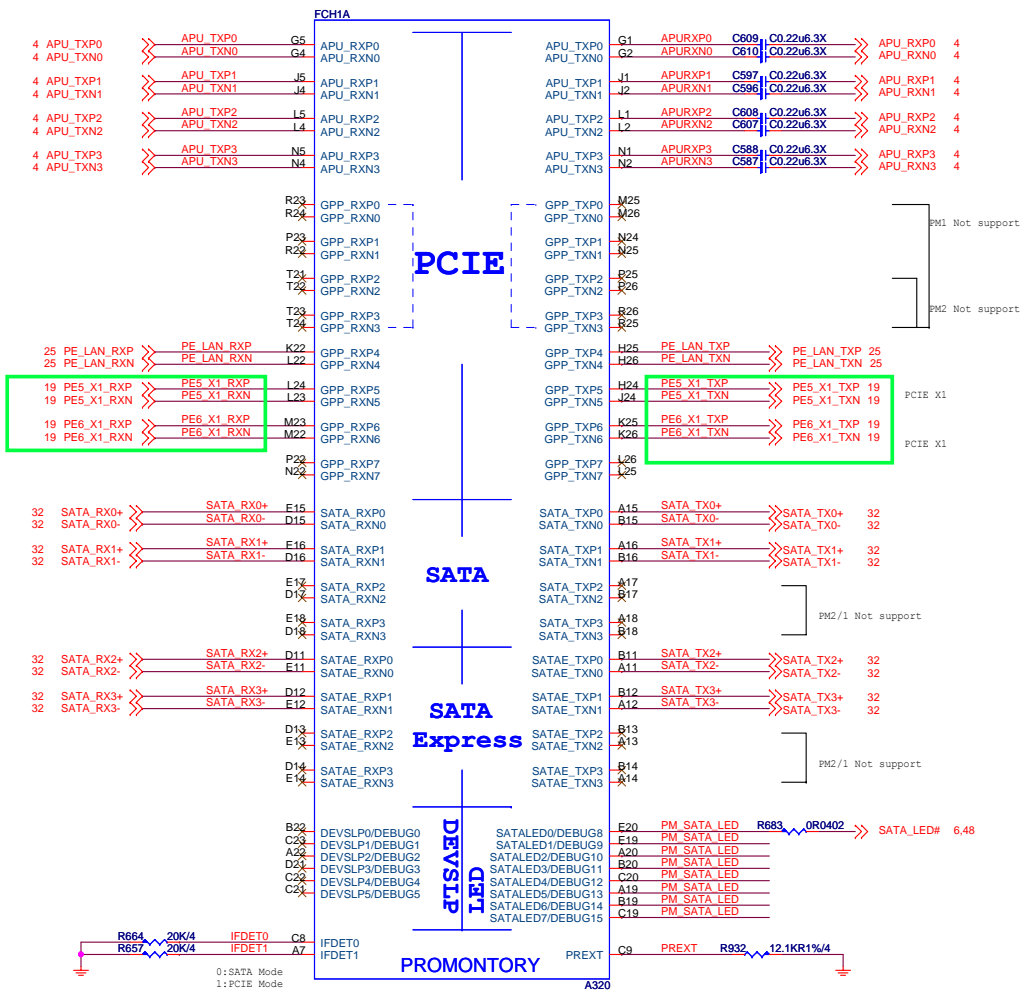




DDR VREF

(place resistors close to DIMMs)

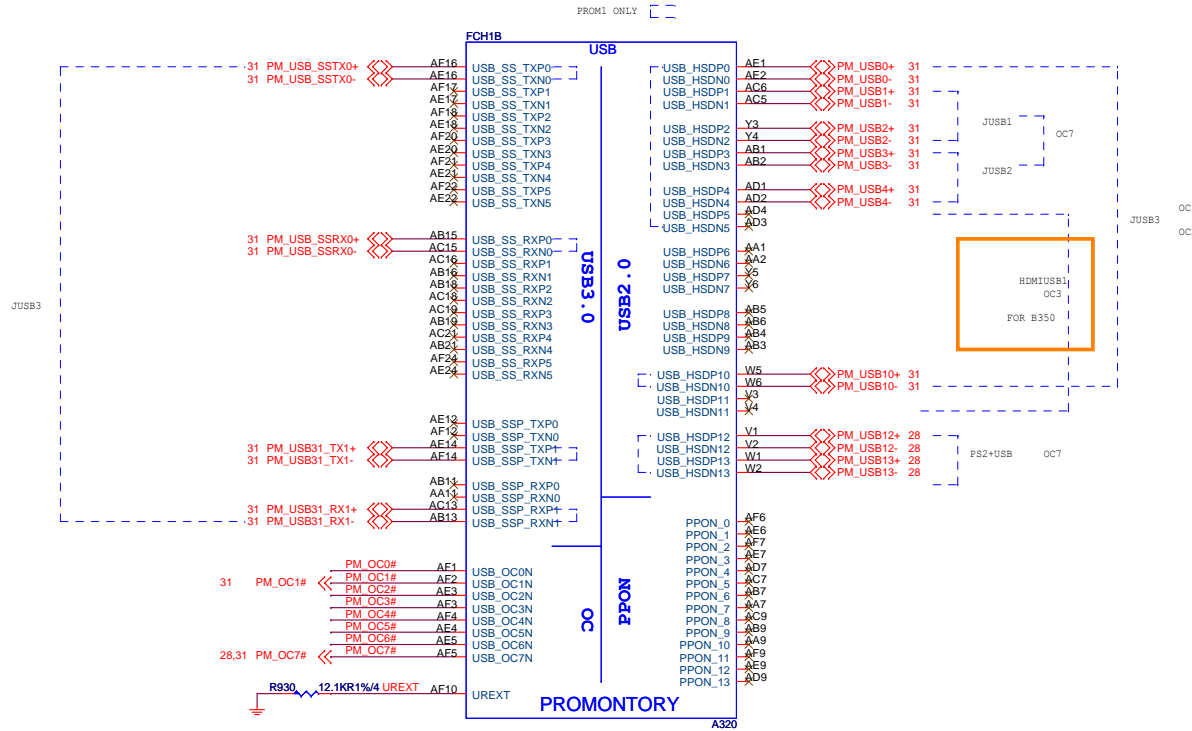
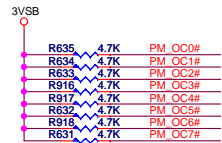


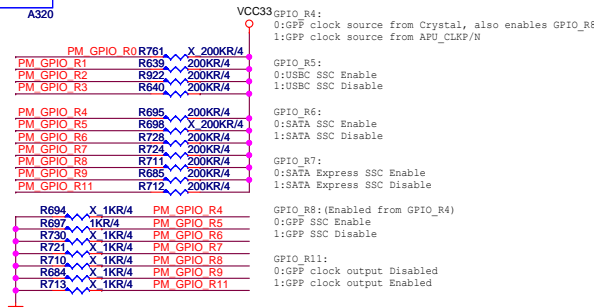
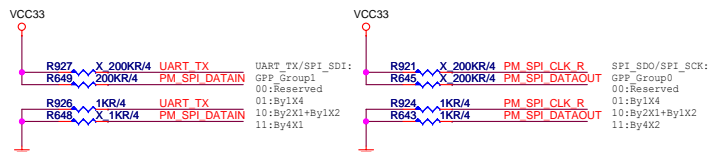
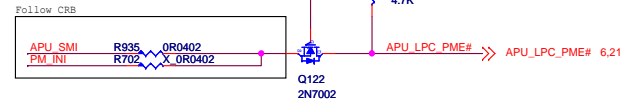
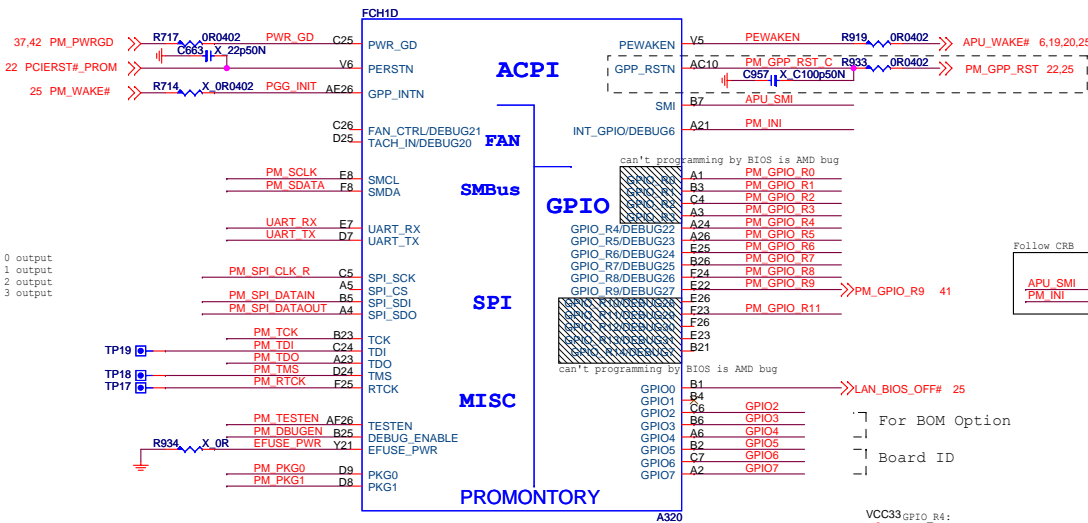
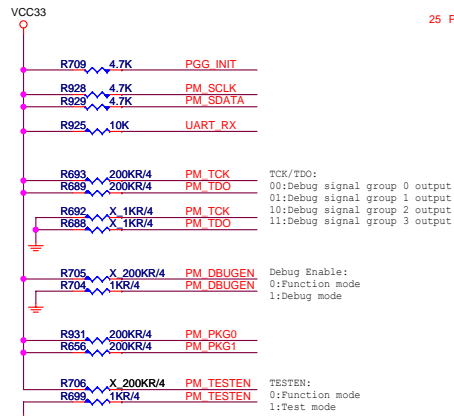
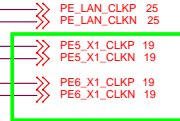
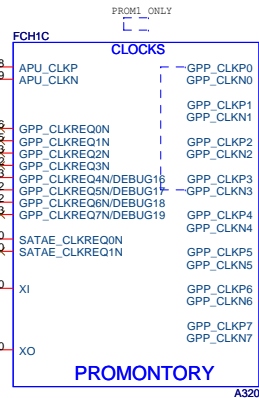
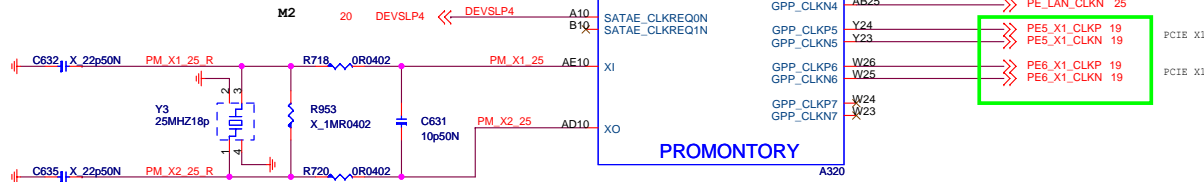
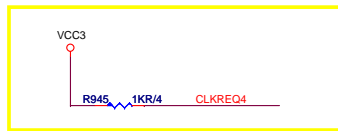


REF1

APRO LED

X_REF1





Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.

BOM OPTION



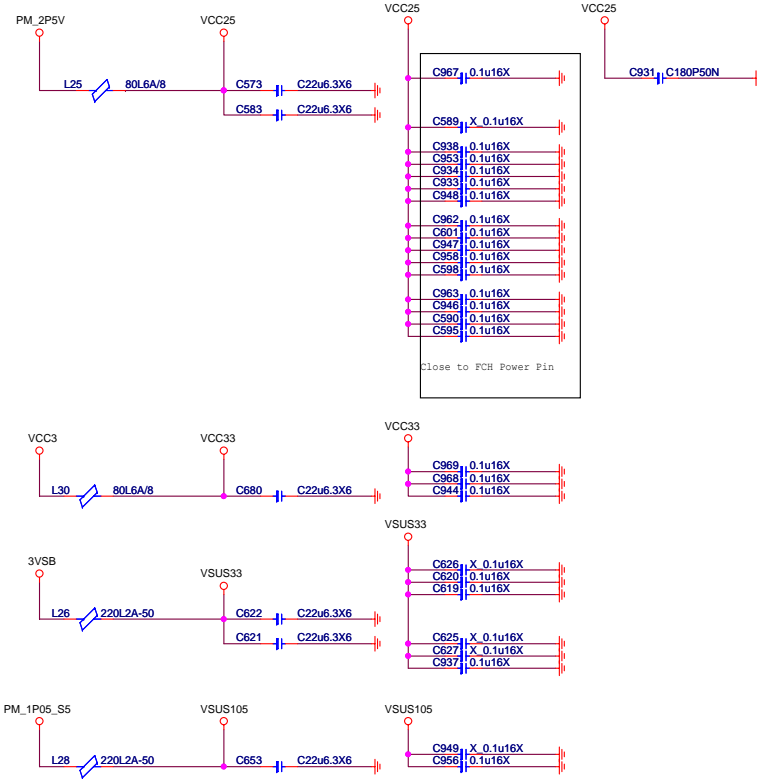
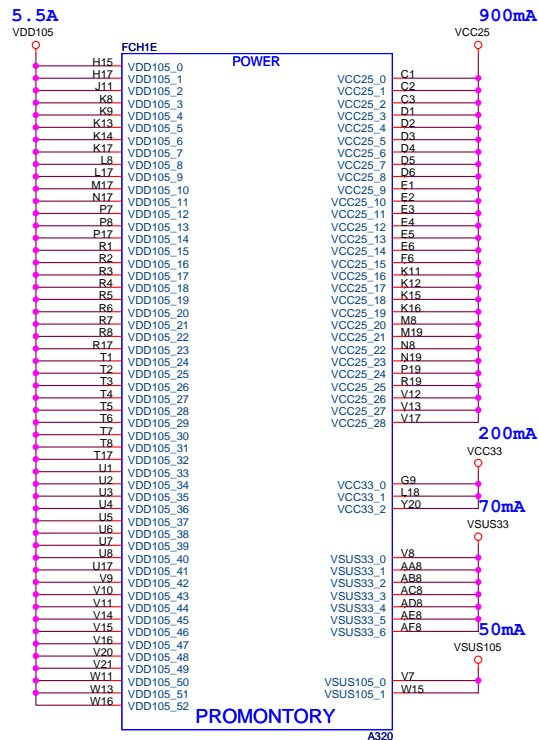
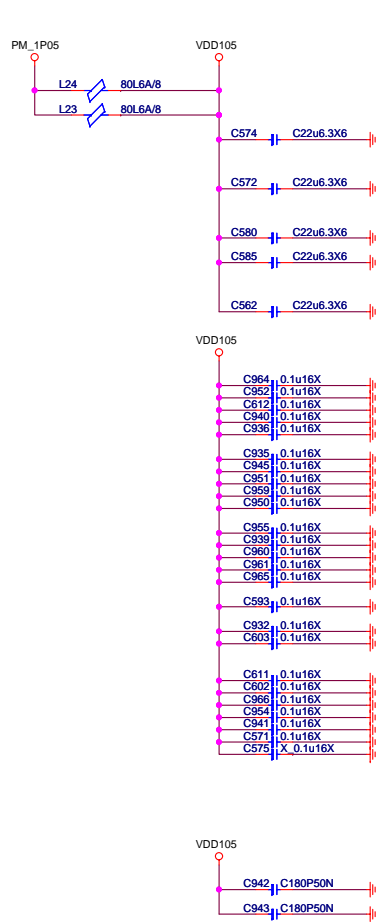
	FULL	
GPIO2	0	
GPIO3	0	
GPIO4	0	



Title: **Promontory-CLK/ACPI/GPIO**

Size: Custom Document Number: **MS-7A39** Rev: **1.0**

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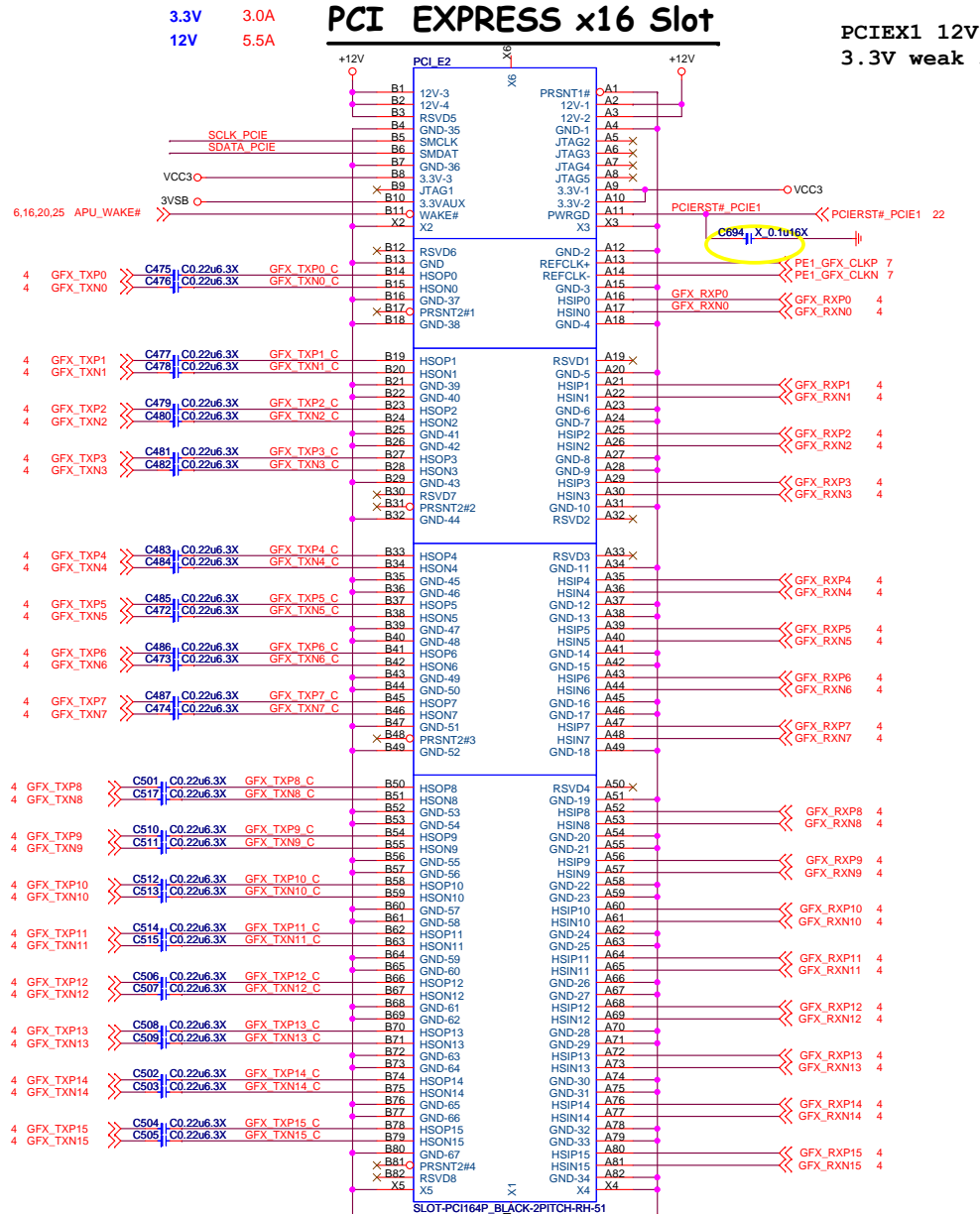
GND

PROMONTORY

PCI EXPRESS x16 Slot

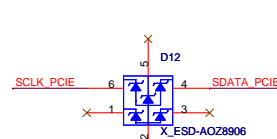
PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V 3.0A
12V 0.5A



PCI Express x16 Slot	
+12V	- 5.5 A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA

SMBus separate circuit



SMB_SEL
GPIO Default High

6 SCLK_PCIE SCLK_PCIE
6 SDATA_PCIE SDATA_PCIE

MICRO-START INT'L CO.,LTD.

Title: **PCIe X16(X1*2) SLOT**

Size: Custom

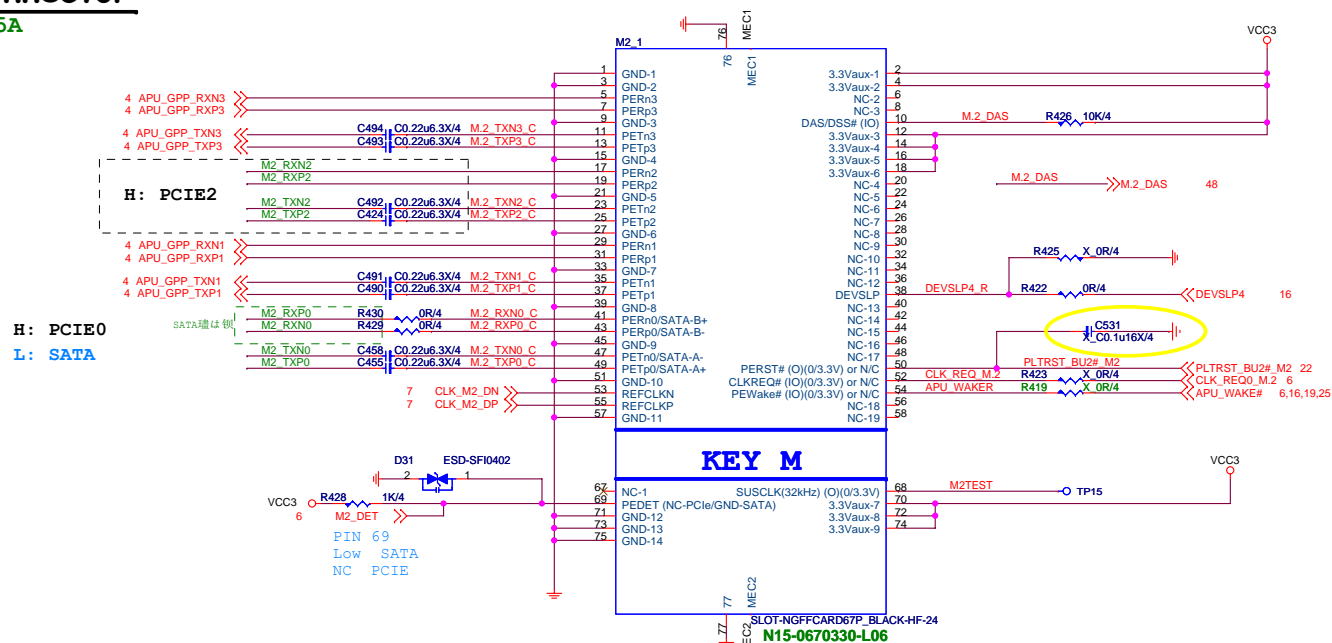
Document Number: **MS-7A39**

Date: Friday, January 20, 2017

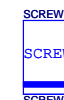
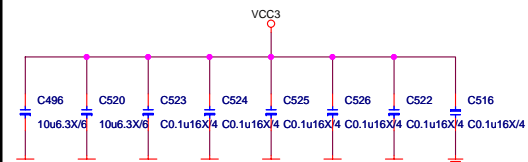
Sheet: 19 of 55

Rev: **1.0**

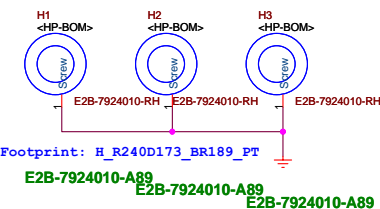
3.3V@2.5A



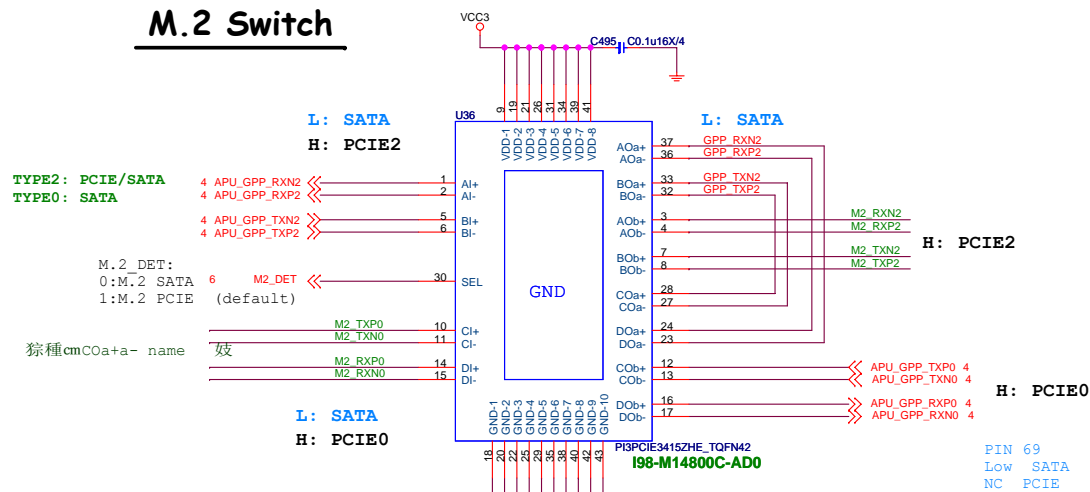
3.3V@2.5A

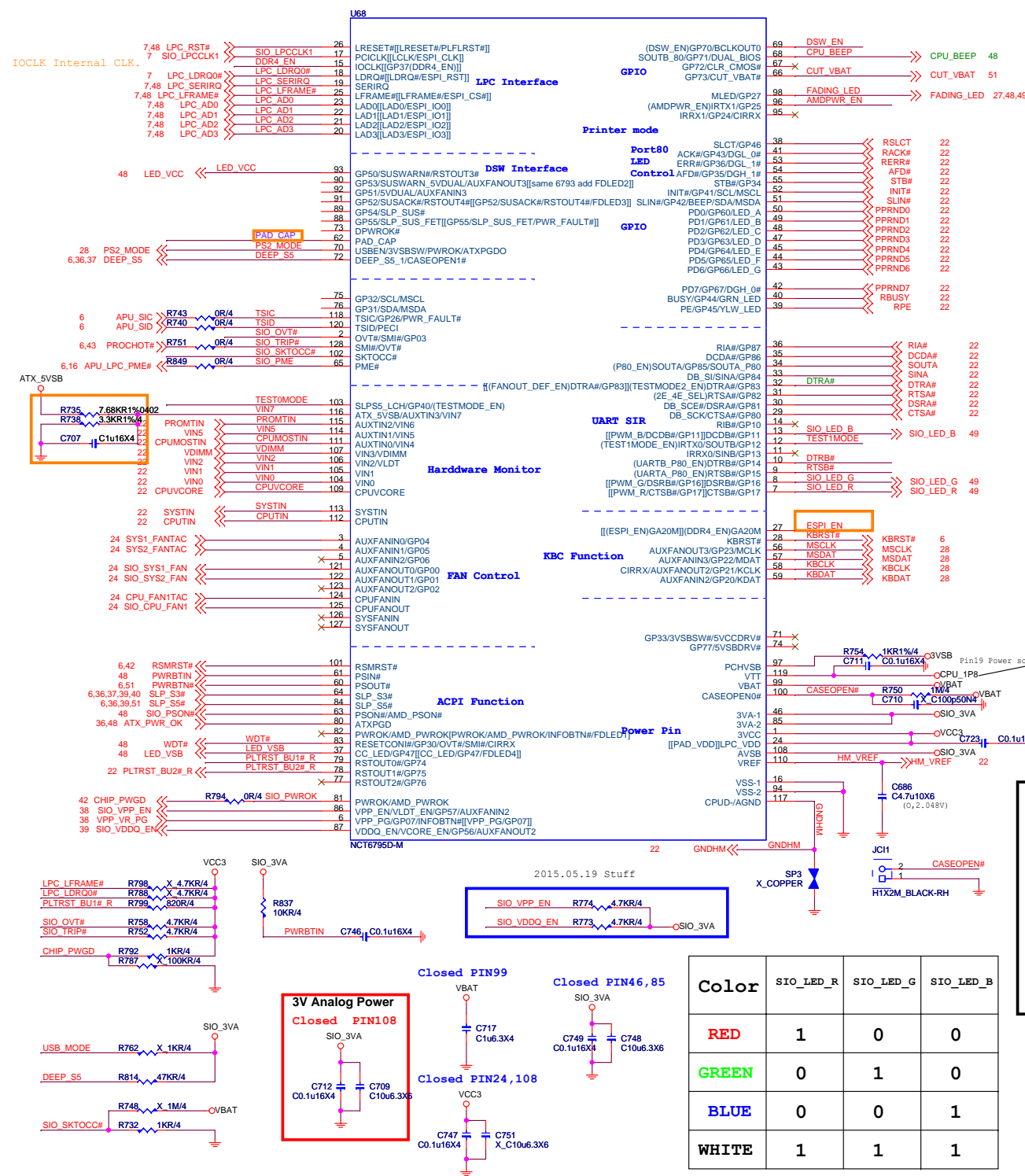


E2B-7984010-A89



M.2 Switch





SIO_3VA

R759 47K/4 FADING_LED

DSW_EN R830 X 0R/4

AMDPWR_EN R755 0R/4

USB_MODE 36

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO

SIO_3VA

R841 1K/4 RTSA#

R840 X 680R/4

R843 X 1K/4 DSW_EN

R822 680R/4

R769 X 1K/4 AMDPWR_EN

R765 680R/4

PAD_CAP

R958 X 680R/4

C974 C4.7u10X6

Co-Lay NCT6795

(PIN9) (RTSB#) 80_ENA 0=Disable 1=Enable

(PIN10) (DTRB#) 80_ENB 0=Disable 1=Enable

(PIN32) (DTRA#) FANOUT 0=50% 1=100%

(PIN12) TEST_MODE_EN1 0=Disable 1=Enable

(PIN103) TEST_MODE_EN0 0=Disable 1=Enable

(PIN27) ESPI_EN0 0=LPC 1=ESPI

(PIN15) DDR4_EN 0=Disable 1=Enable

SIO_3VA

R772 1K/4 DDR4_EN

R778 X 1K/4

R805 1K/4

R766 X 1K/4 RTSB#

R771 680R/4

R770 X 1K/4 DTRB#

R777 680R/4

R821 1K/4 DTRA#

R829 X 680R/4

TEST1MODE R783 680R/4

TESTMODE R744 680R/4

SIO_3VA

R545 10K/1% SIO_LED_R

R790 X 100K/4

SIO_3VA

R546 X 10K/1% SIO_LED_G

R789 100K/4

SIO_3VA

R548 X 10K/1% SIO_LED_B

R791 100K/4

MSI

Link to the Future

MICRO-START INT'L CO.,LTD.

Title: **SIO NCT5565**

Size: Document Number **MS-7A39**

Custom: Rev **1.0**

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Inform BIOS disable VIN2 with Power Fault

VCCP_NB ○ R532 10KR1%4 VIN2

R542 X_10KR1%4

C547 10u6.3X/6

CPU_VDDP ○ R541 10KR1%4 VIN5

C555 10u6.3X/6

VCORE ○ R374 10KR1%4

C359 10u6.3X/6

VCC_DDR ○ R534 10KR1%4

C558 10u6.3X/6

VCCP_NB CPU_VDDP VCORE VCC_DDR

For CPU Under Socket

HM_VREF 21

R722 10K1%

CPUTIN 21

RT6 10KRT1%0402

C685 C2200p50X

GNDHM 21

For System Close to SIO

SYSTIN 21

Q53 P-3906

C488 2.2n50X/4

GNDHM

Close to CPU MOS

HM_VREF 21

R551 10KRT1%4

PROMTIN 21

RT2 10KRT1%0402

C533 C2200p50X/4

GNDHM 21

Close to CPU MOS

[illegible]

The schematic diagram illustrates the electrical connections for the N31-21M131-H06 board. At the top, a D45 1N4148W diode is connected between VCC5 and LPT_VG. A capacitor C656 (C0.1u16X/4) is connected to LPT_VG. The diagram shows various components connected to the J1LPT1 connector pins, including resistors (R707-R782), diodes (D45), and capacitors (C637-C690). The components are organized into groups corresponding to the connector pins, with labels for each component and its value. The diagram also shows the connection of the J1LPT1 connector to the board, with pins 1 through 25 labeled. The board is identified as H2XT3[28]M_BLACK-RH N31-21M131-H06.

Component List:

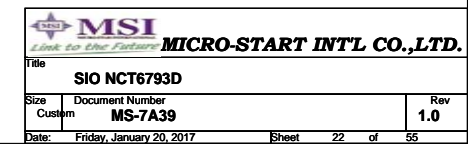
- D45 1N4148W
- C656 C0.1u16X/4
- R707 33R/4
- R736 33R/4
- R760 33R/4
- R700 33R/4
- R701 33R/4
- R733 33R/4
- R746 33R/4
- R780 33R/4
- R725 33R/4
- R745 33R/4
- R757 33R/4
- R782 33R/4
- R716 2.7K/4
- R727 2.7K/4
- R741 2.7K/4
- R763 2.7K/4
- R719 2.7K/4
- R739 2.7K/4
- R749 2.7K/4
- R781 2.7K/4
- R726 2.7K/4
- R747 2.7K/4
- R767 2.7K/4
- R784 2.7K/4
- R729 2.7K/4
- R756 2.7K/4
- R775 2.7K/4
- R723 2.7K/4
- R715 2.7K/4
- C637 X 470p50/4
- C641 X 470p50/4
- C652 X 470p50/4
- C639 X 470p50/4
- C643 X 470p50/4
- C644 X 470p50/4
- C654 X 470p50/4
- C640 X 470p50/4
- C642 X 470p50/4
- C651 X 470p50/4
- C657 X 470p50/4
- C638 X 470p50/4
- C650 X 470p50/4
- C655 X 470p50/4
- C659 X 470p50/4
- C649 X 470p50/4
- C660 X 470p50/4

Connector Pin List:


- 1 RSTB#
- 2 PRND0
- 3 PRND1
- 4 PRND2
- 5 PRND3
- 6 PRND4
- 7 PRND5
- 8 PRND6
- 9 PRND7
- 10 RACK#
- 11 RBUSY
- 12 RPE
- 13 RSLCT
- 14 RERR#
- 15 RSTB#
- 16 PRND0
- 17 PRND1
- 18 PRND2
- 19 PRND3
- 20 PRND4
- 21 PRND5
- 22 PRND6
- 23 PRND7
- 24 RACK#
- 25 RBUSY

Board Identification:

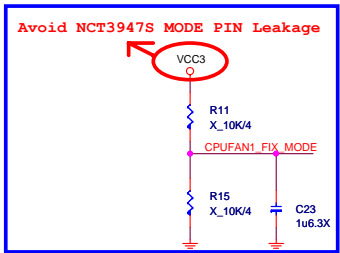
H2XT3[28]M_BLACK-RH
N31-21M131-H06



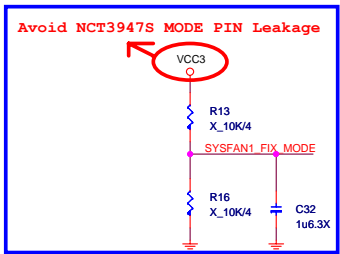
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D				D
C				C
B				B
A				A

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Title Manual parts		
Size Custom	Document Number MS-7A39	Rev 1.0
Date: Tuesday, January 03, 2017	Sheet 23	of 55

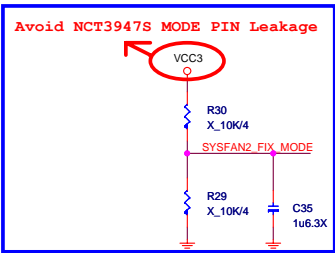
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE
2.GPIO バイオス伝 PWM/DC MODE



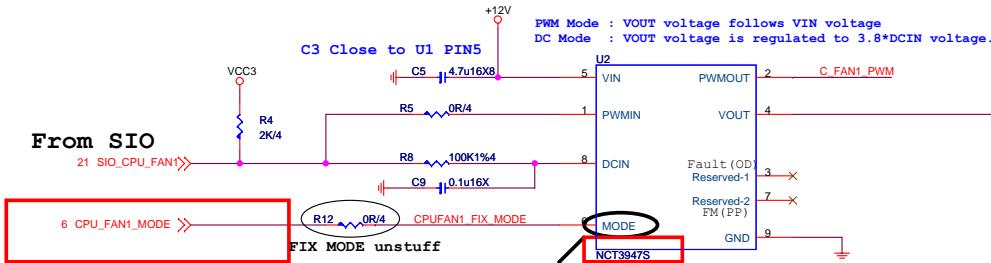
Resever For FIX DC or PWM MODE USE By PM SPEC



Resever For FIX DC or PWM MODE USE By PM SPEC

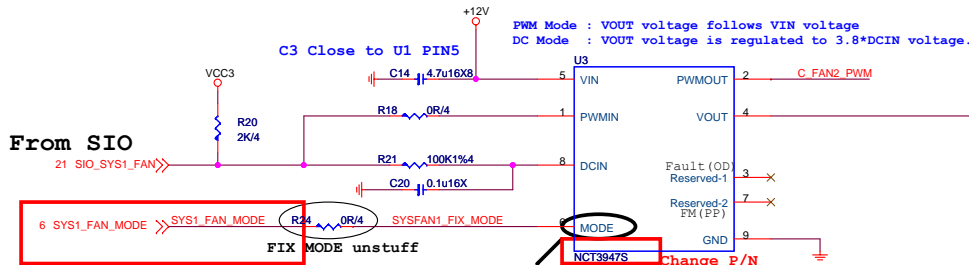
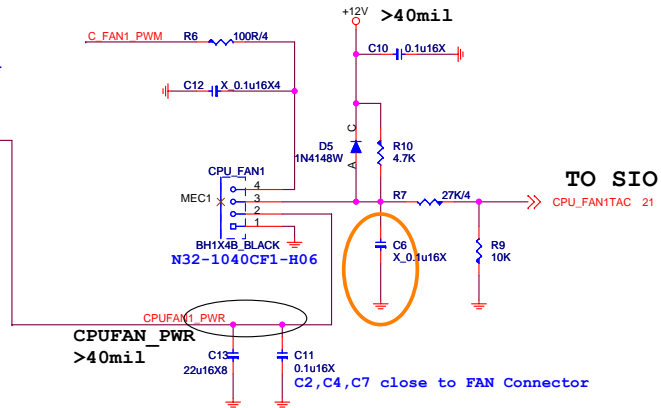


Resever For FIX DC or PWM MODE USE By PM SPEC



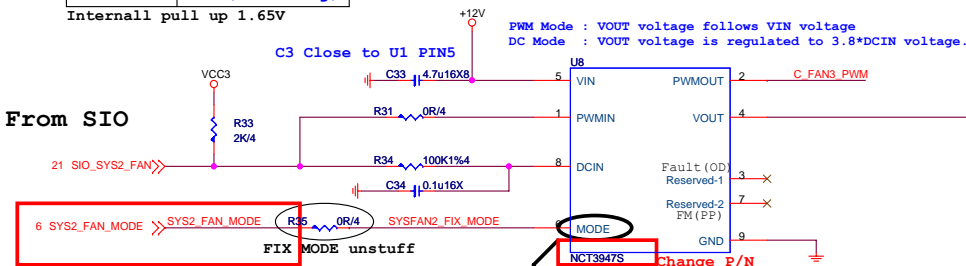
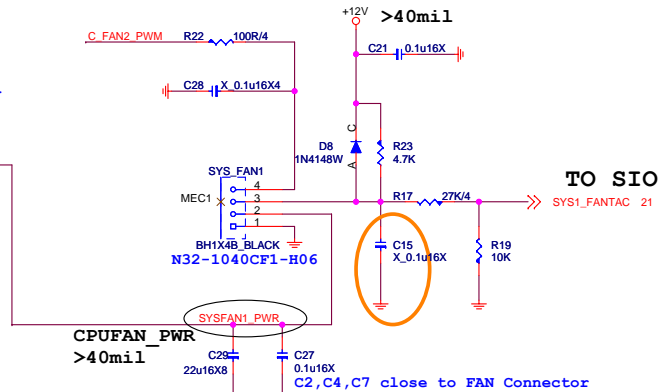
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Internall pull up 1.65V



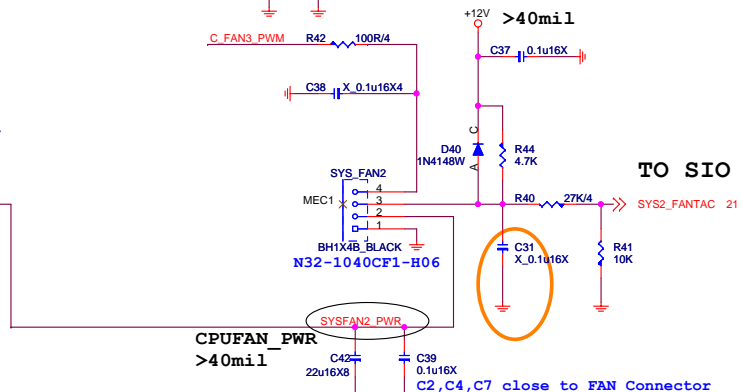
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Internall pull up 1.65V

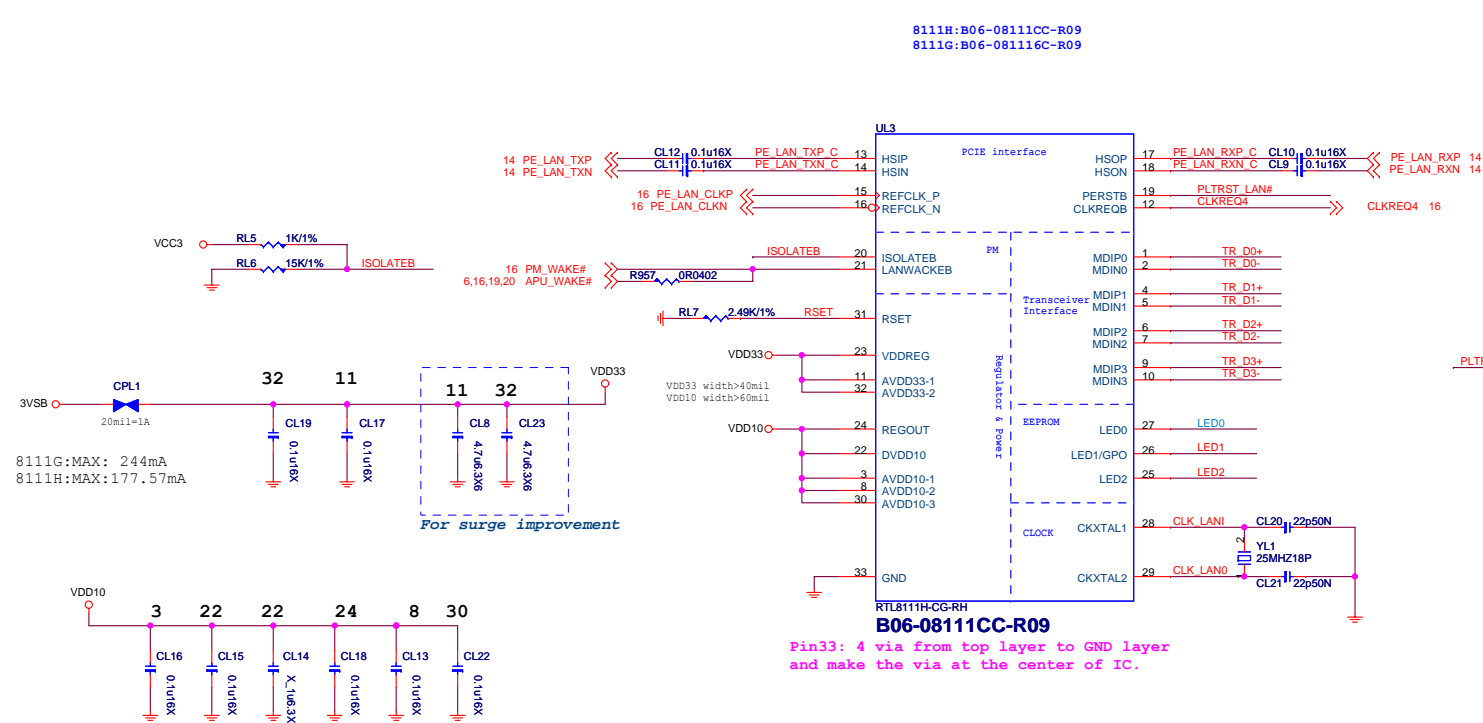


	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Internall pull up 1.65V



RTL8111G/RTL8111H Giga LAN



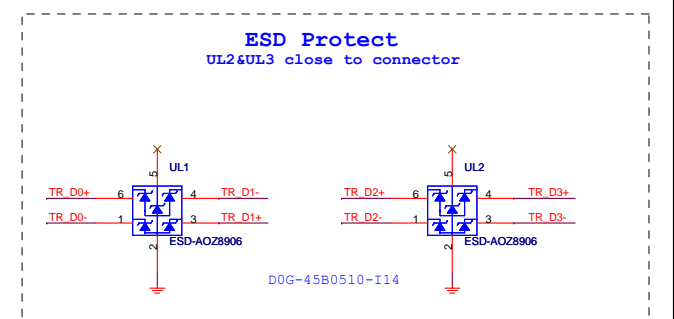
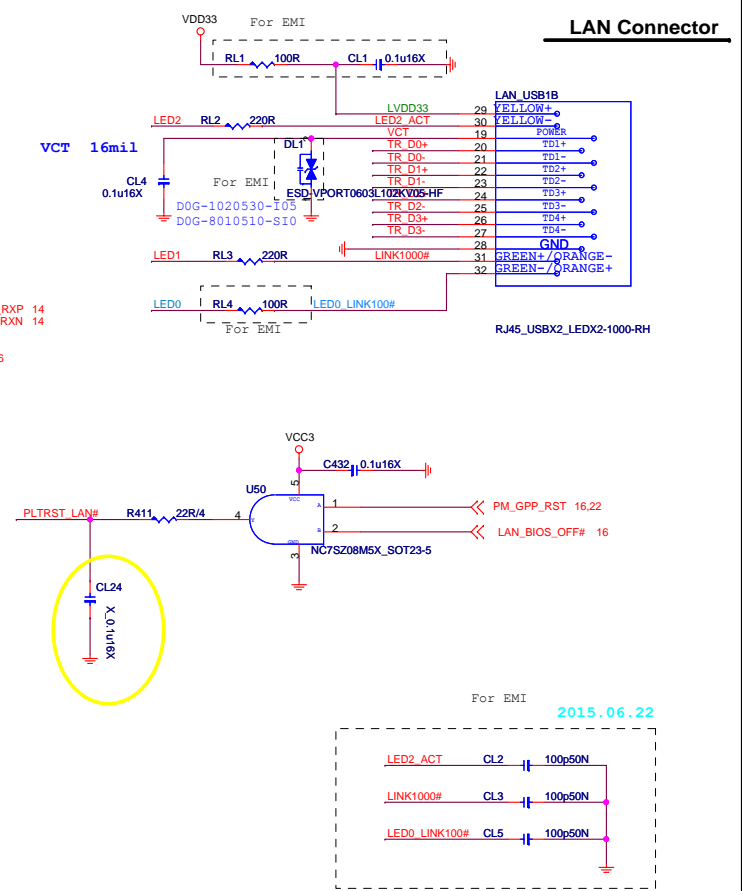
8111G:MAX: 244mA
8111H:MAX:177.57mA

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

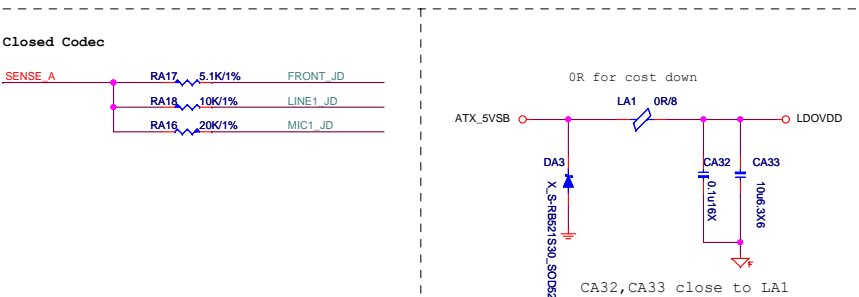
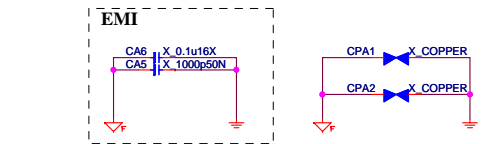
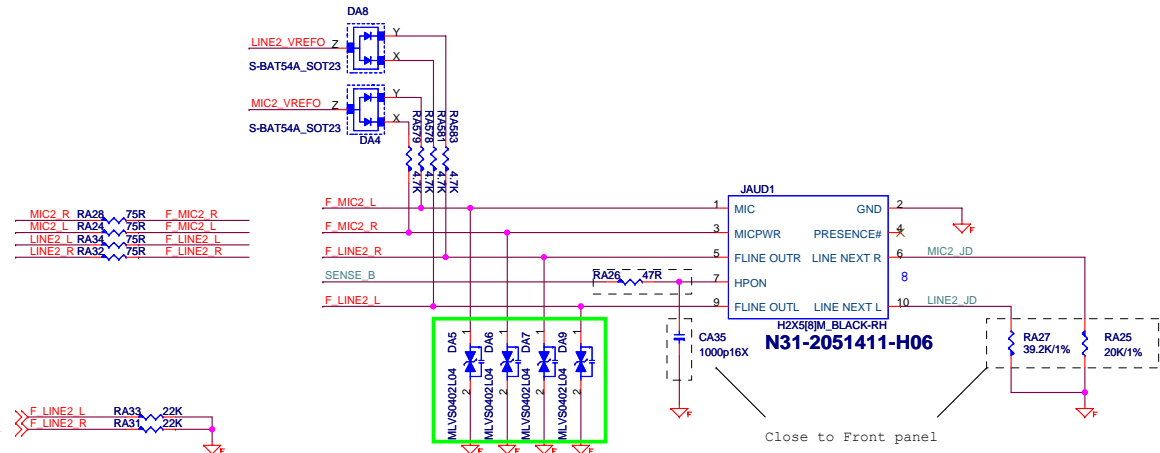
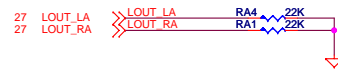
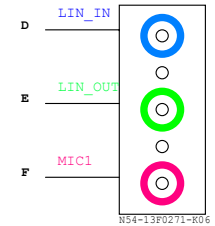
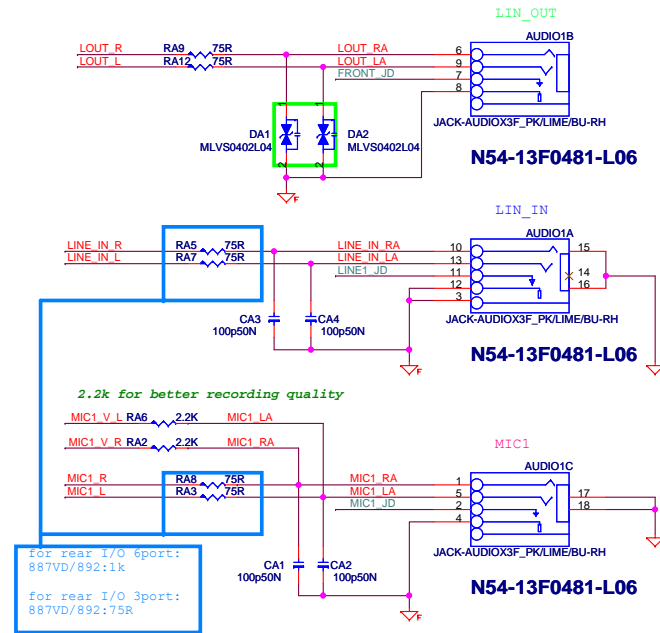
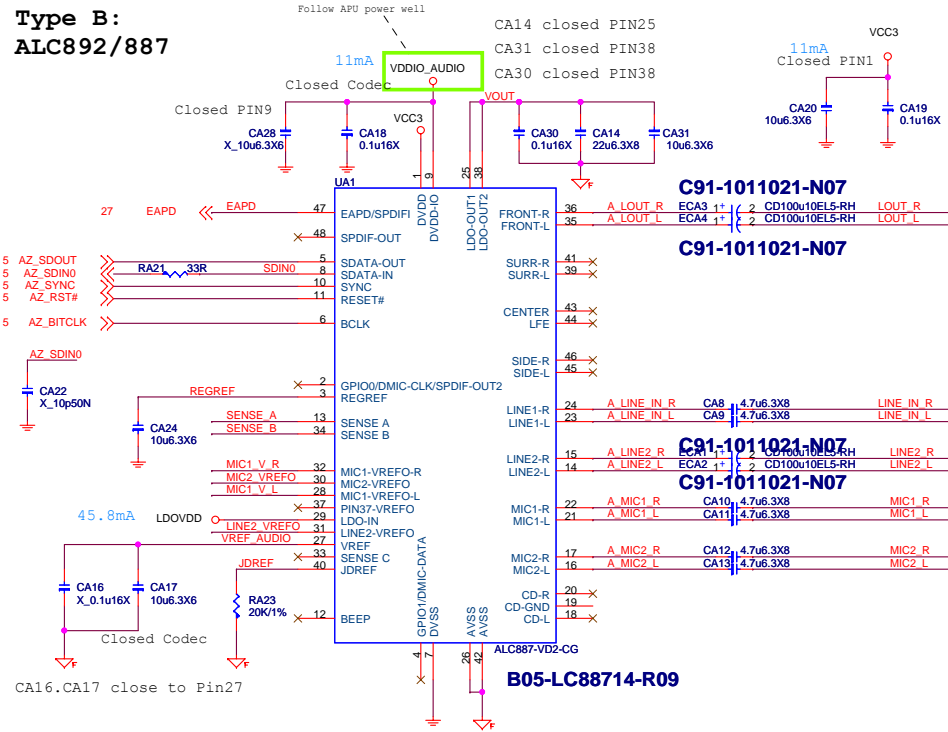
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Size: Custom
Document Number: **MS-7A39**

Date: Friday, January 20, 2017
Sheet: 25 of 55

Rev: **1.0**

Type B:
ALC892/887

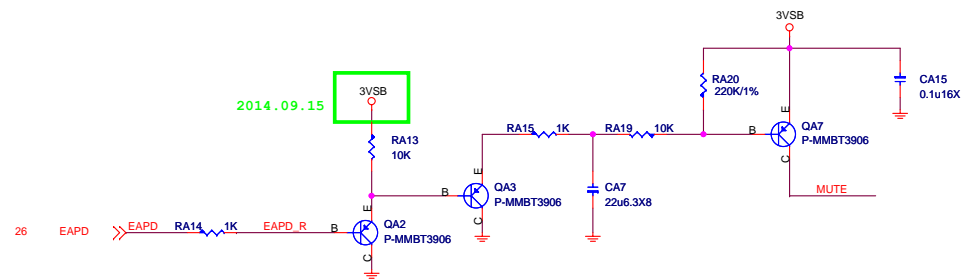


Varister --> cap for cost down
D0G-2710510-I05
D0G-2950500-SI0
Close to Jack

Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

2014.09.15

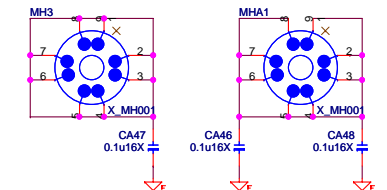
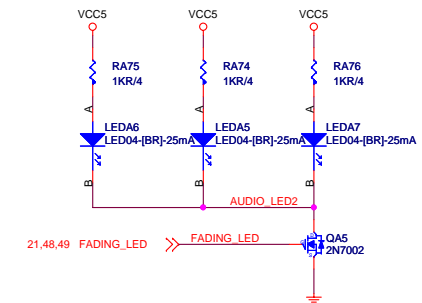
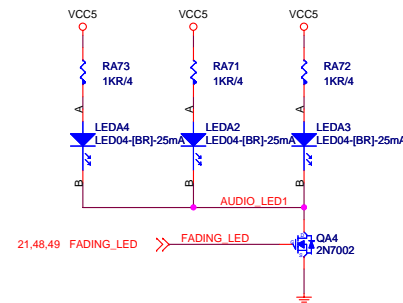


Digital

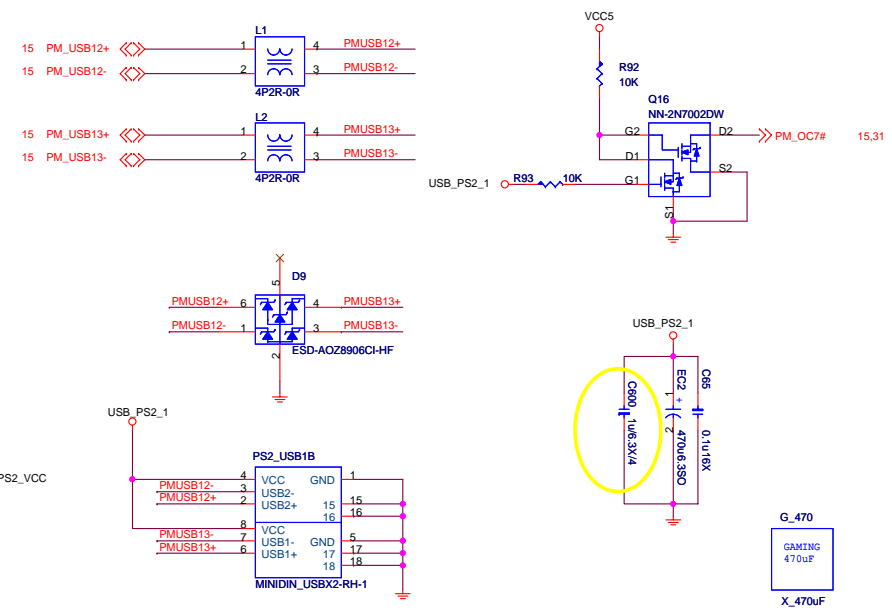
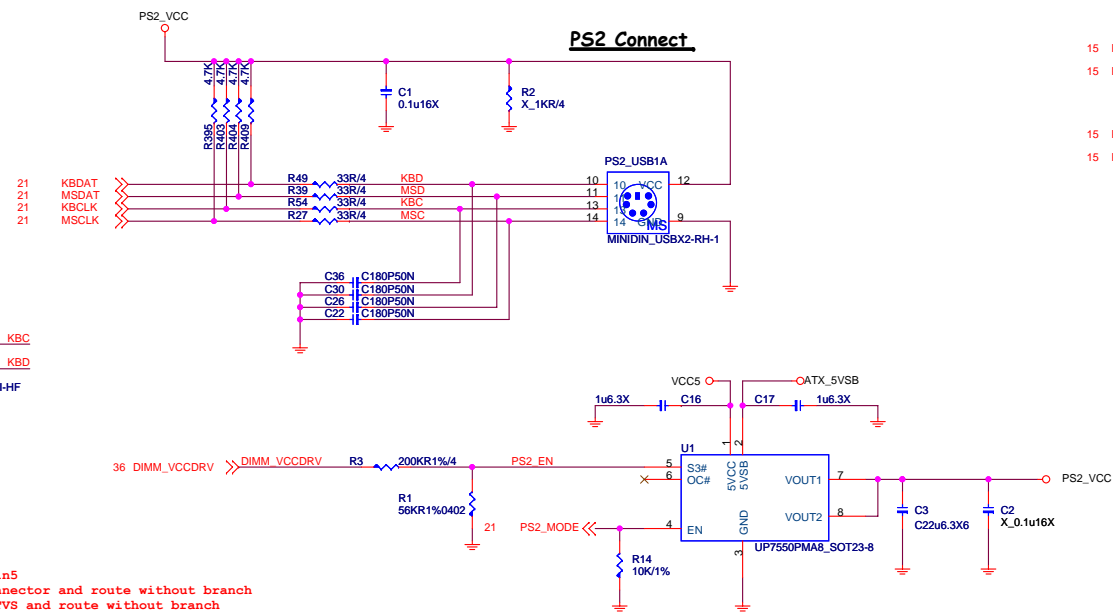
Analog



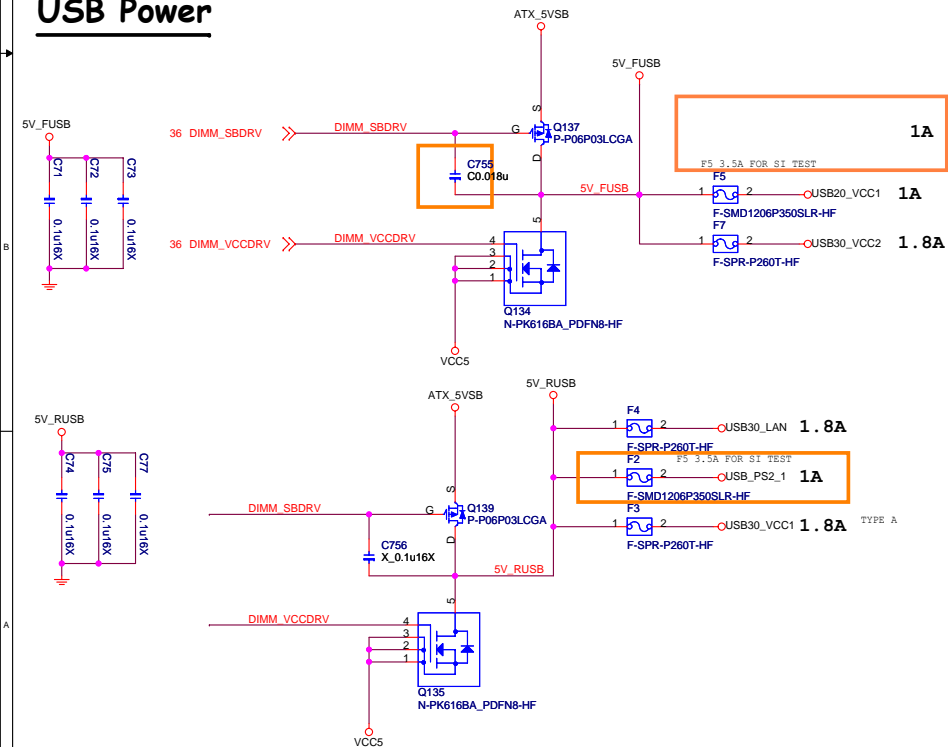
厂代 LED



PS2+USB

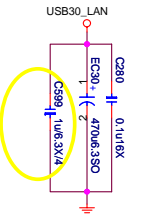
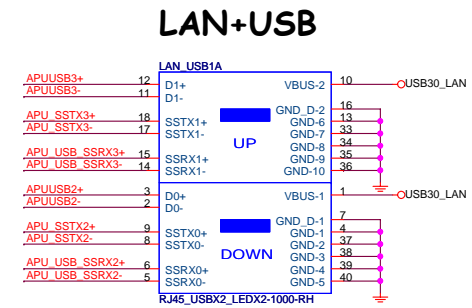
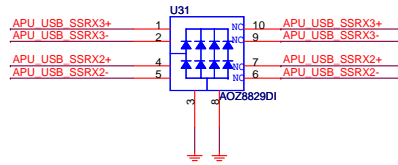
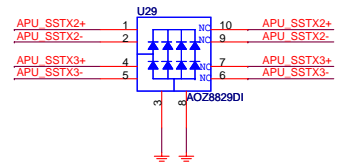
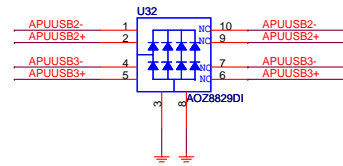
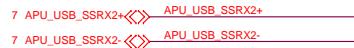
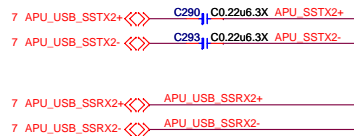
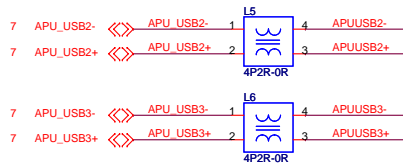


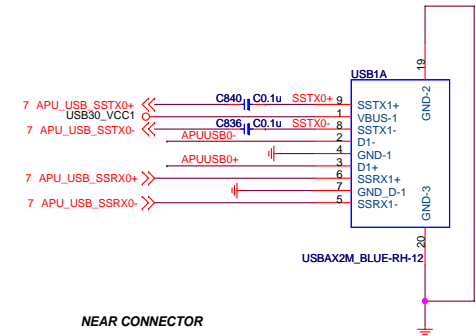
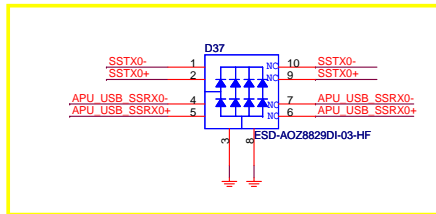
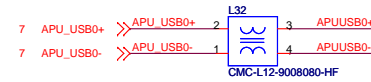
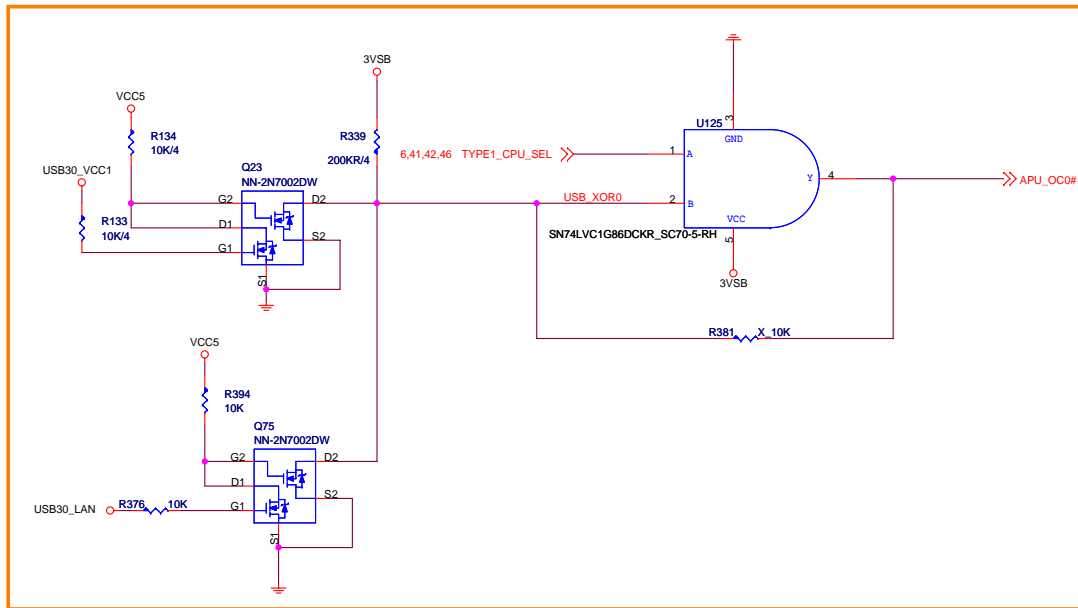
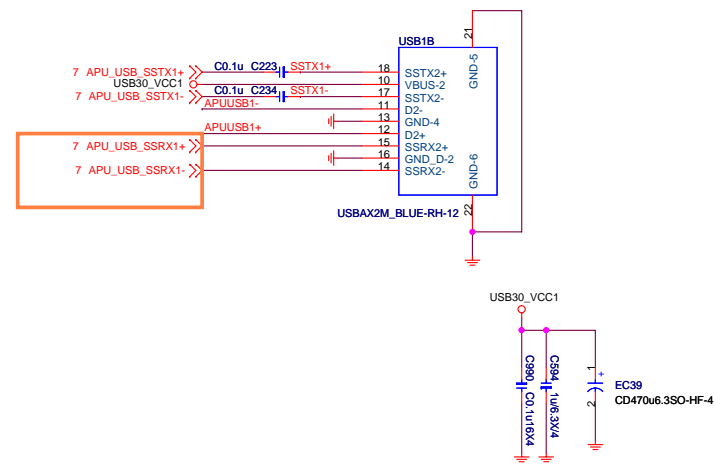
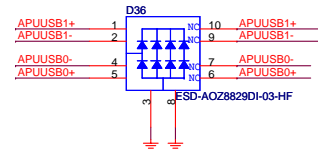
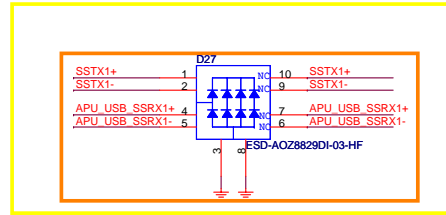
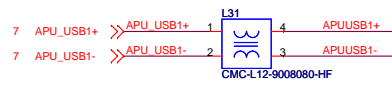
USB Power



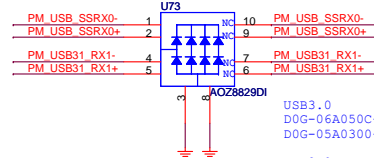
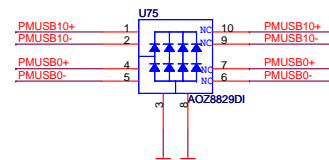
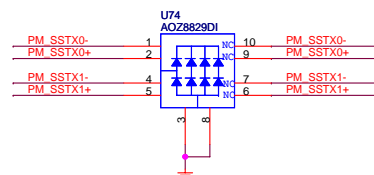
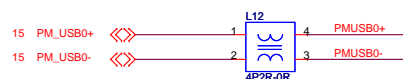
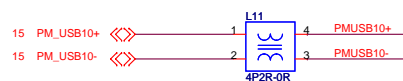
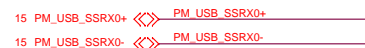
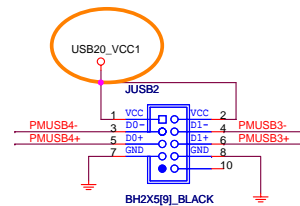
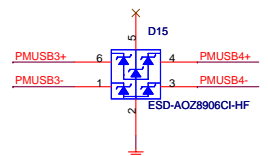
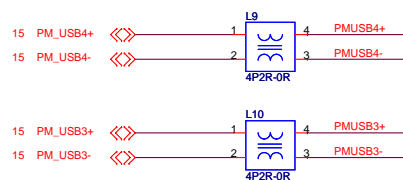
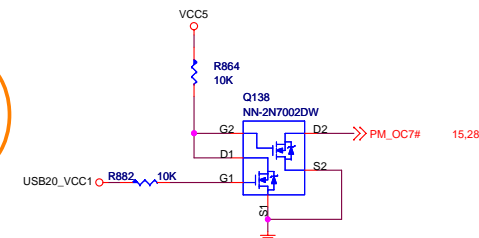
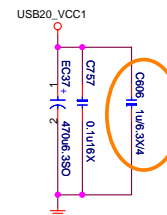
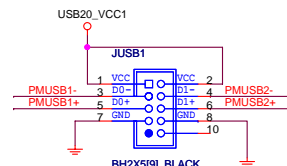
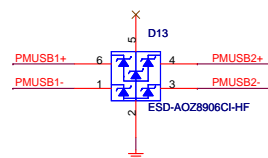
USB3.1 GEN1

VR Sloution U2 redriver





5	4	3	2	1
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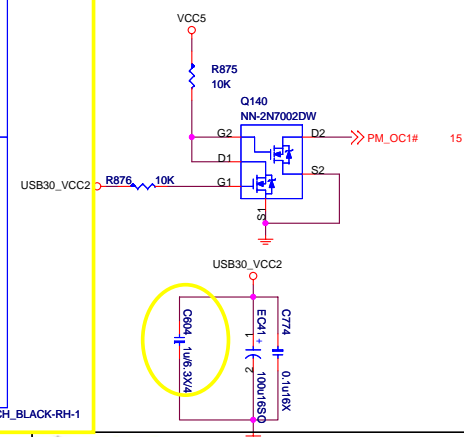
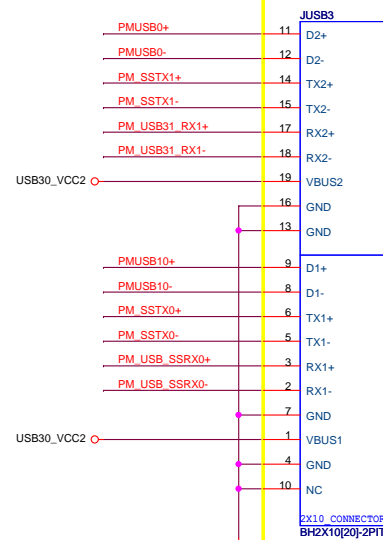


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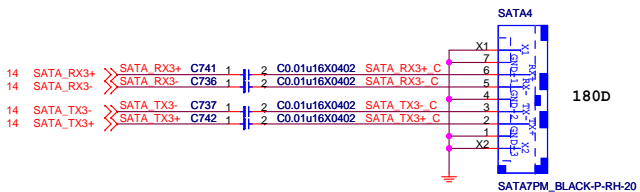
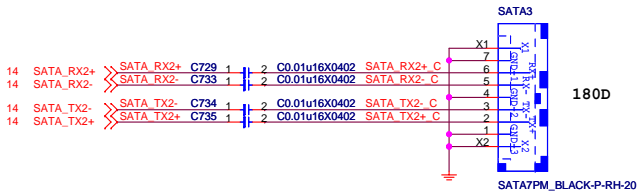
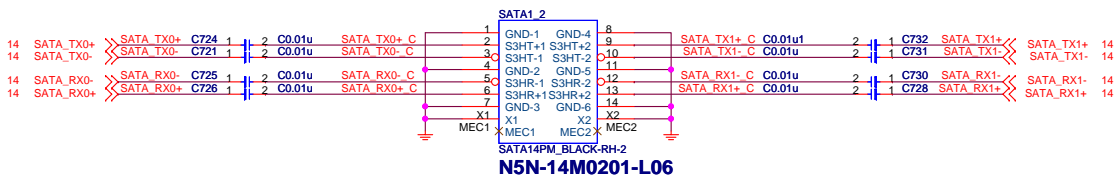
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL

```



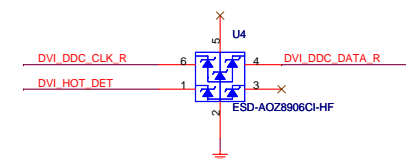
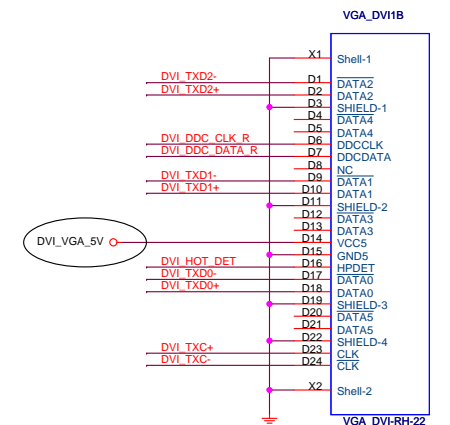
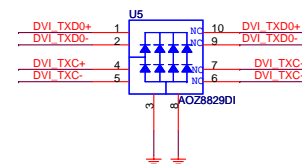
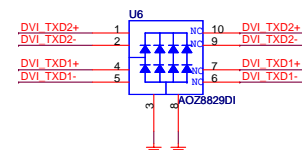
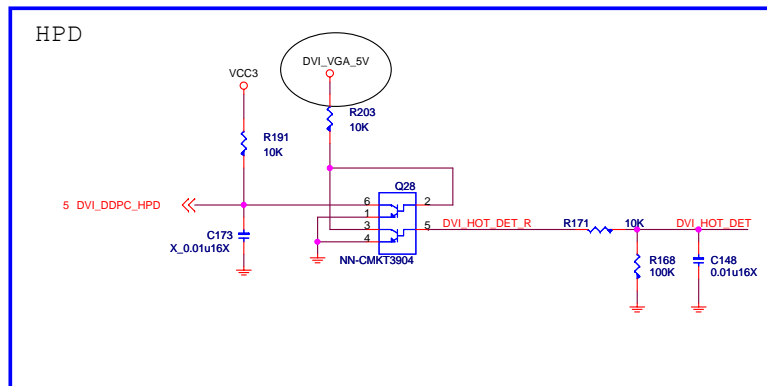
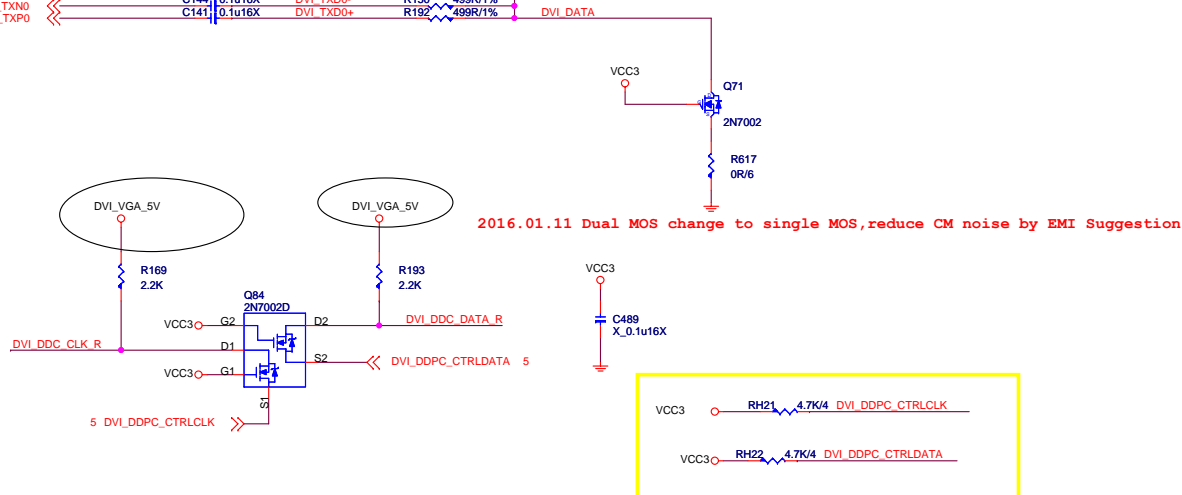
SATA Connector



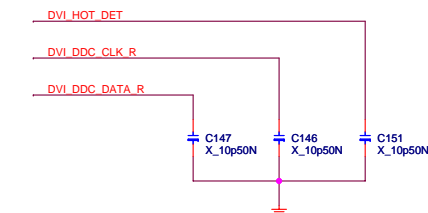
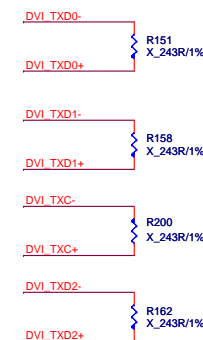
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

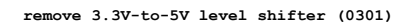
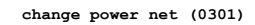
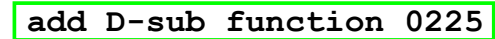
5 DVI_DDPC_CLK_N	C154	0.1u16X	DVI_TXC-	R165	499R/1%
5 DVI_DDPC_CLK_P	C159	0.1u16X	DVI_TXC+	R201	499R/1%
5 DVI_DDPC_TXN2	C149	0.1u16X	DVI_TXD2-	R194	499R/1%
5 DVI_DDPC_TXP2	C171	0.1u16X	DVI_TXD2+	R164	499R/1%
5 DVI_DDPC_TXN1	C169	0.1u16X	DVI_TXD1-	R207	499R/1%
5 DVI_DDPC_TXP1	C143	0.1u16X	DVI_TXD1+	R160	499R/1%
5 DVI_DDPC_TXN0	C144	0.1u16X	DVI_TXD0-	R150	499R/1%
5 DVI_DDPC_TXP0	C141	0.1u16X	DVI_TXD0+	R192	499R/1%



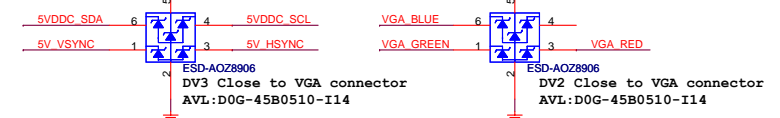
For EMI



If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



The diagram shows two horizontal timelines. The top timeline is for HSYNC, with labels HSYNC, RV16, 33R/4, and 5V_HSYNC. The bottom timeline is for VSYNC, with labels VSYNC, RV20, 33R/4, and 5V_VSYNC. Both timelines have a blue zigzag line representing a clock signal between the RV and 33R/4 labels.



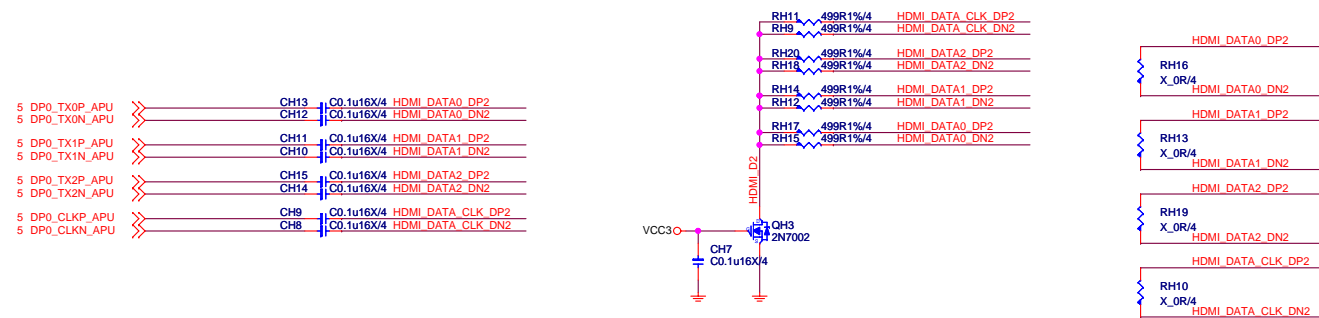
100 ohm change to 22 ohm (0301)

Vendor suggest 22ohm for better I2C quality

DVI_PRO

X_DVI_APRO

For HDMI 1.4



$I_B = (V_{CC5} - V_{be}) / 10k$
 $(5 - 0.95) / 10k = 0.405mA$
 $I_C = (V_{CC3} - V_{ce}) / 4.7k$
 $(3.3 - 0.2) / 4.7k = 0.659mA$

$I_B = (V_{CC5} - V_{be}) / 10k$
 $(5 - 0.95) / 10k = 0.405mA$
 $I_C = (V_{CC5} - V_{ce}) / 10k$
 $(5 - 0.2) / 10k = 0.48mA$

+12V
 R98 10K/4
 VCC5V
 Q17 N-QM3010K, SOT23-3-HF
 F-MICROMD110
 1 2
 HDMI_PWR_5V
 D08-0100200-B07
 柵ノDIODE SA代剛笨潰積い 笛

HDMI1

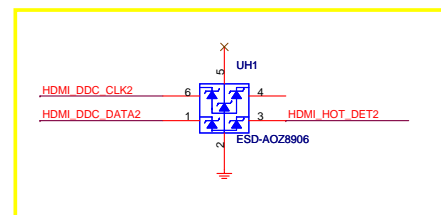
1 TMDs Data+
2 TMDs Data2 Shield
3 TMDs Data2-
4 TMDs Data+
5 TMDs Data1 Shield
6 TMDs Data1-
7 TMDs Data0+
8 TMDs Data0 Shield
9 TMDs Data0-
10 TMDs Clock+
11 TMDs Clock Shield
12 TMDs Clock-
13 CSC
14 Utility
15 SCL
16 SDA
17 DDC/CSC Ground
18 +5V Power
19 Hot Plug Detect

HDMI DATA DP2
HDMI DATA1 DP2
HDMI DATA0 DP2
HDMI DATA0 DN2
HDMI DATA CLK DP2
HDMI DATA CLK DN2
HDMI DDC CLK2
HDMI DDC DATA2
HDMI_PWR_5V
HDMI_HOT_DET2

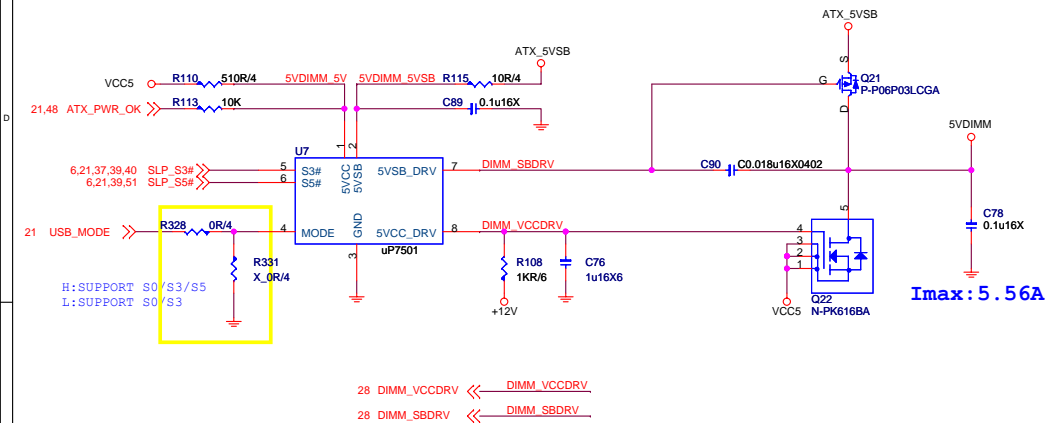
CH3 C0.1u16X/6
CH2 10u6.3X/6

HDMI19PM_BLACK-HF-3
N5Y-19M0721-L06

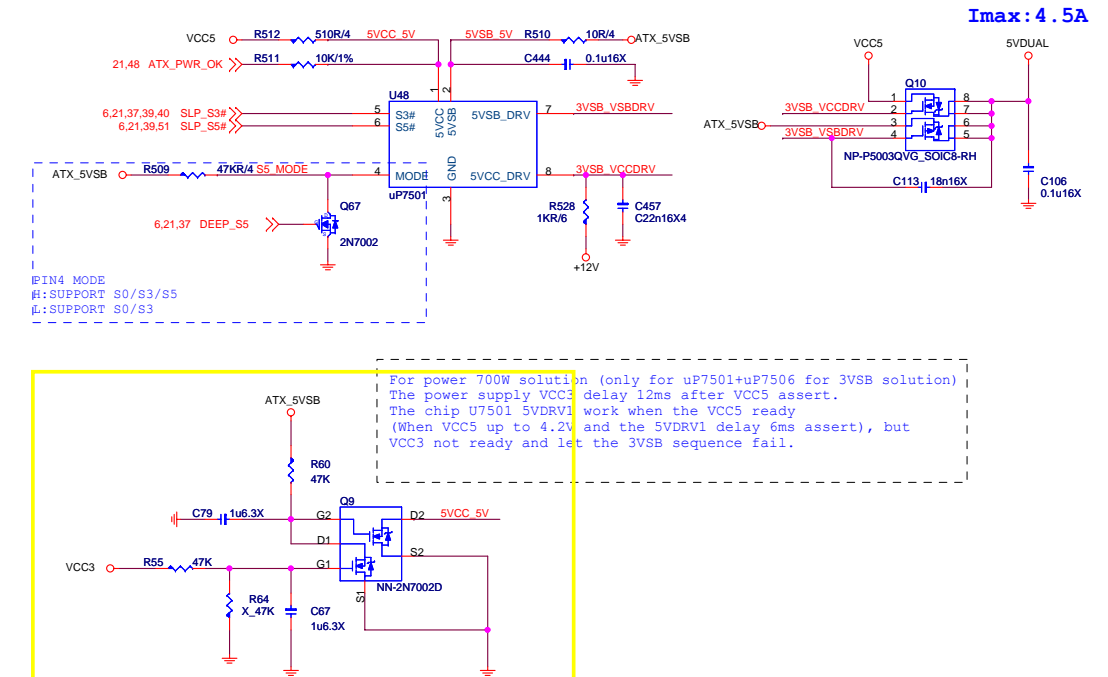
X1
X4
MEC1
X3
X2



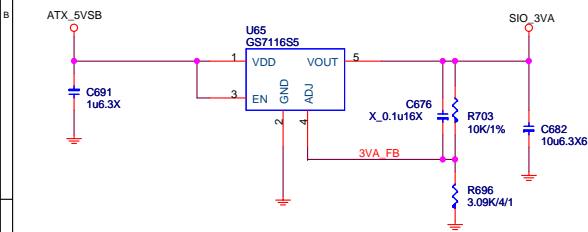
5VDIMM FOR DDR



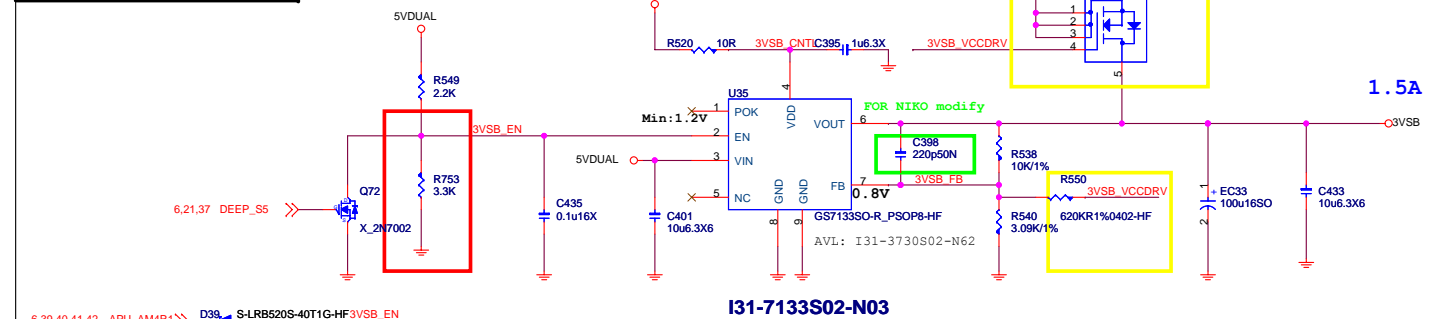
5VDUAL For 3VSB CPU 1.8V VDDP



SIO_3VA



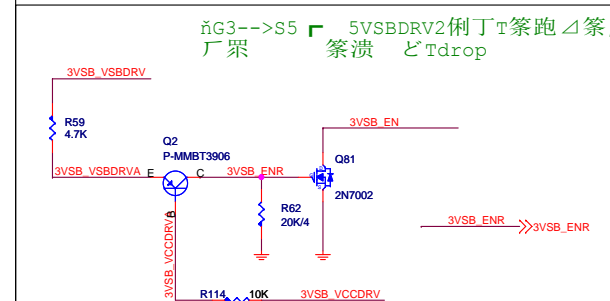
3VSB cost down



3VSB cost down

3.3V@1.4959A

1.05V@0.05A
VDDBT_RTC_G@4.5uA
FCH@0.07A
CPU@0.25A
PCI-E*3 @1.125A
USB TYPE-C @0.9mA



1.05V
S0:5.5A
S5:0.05A

support OV=>NB685
not support OV=> NB681

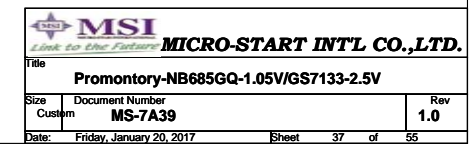
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

$$0.7776\mu H \leq L \leq 1.1664\mu H$$

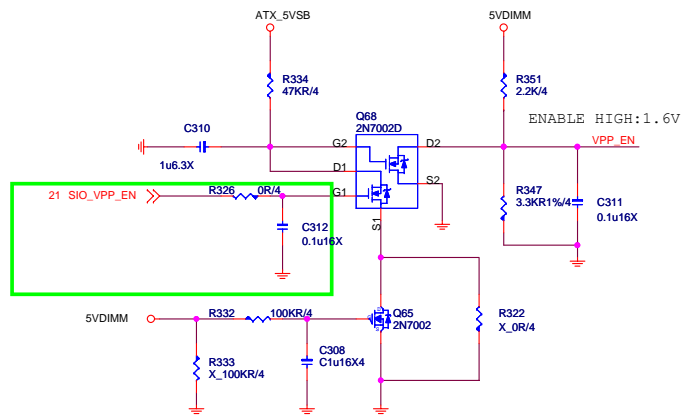
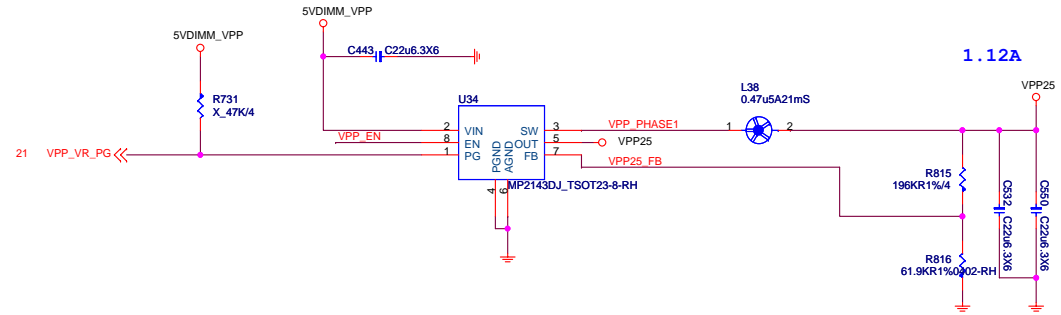
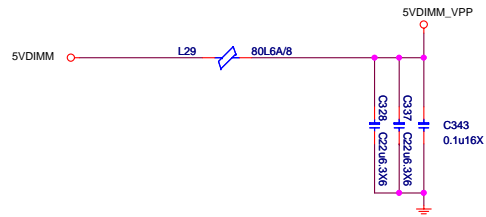

0.05A



2.5V; 900mA



2DIMM :1.12A FOR DDR VPP2.5V

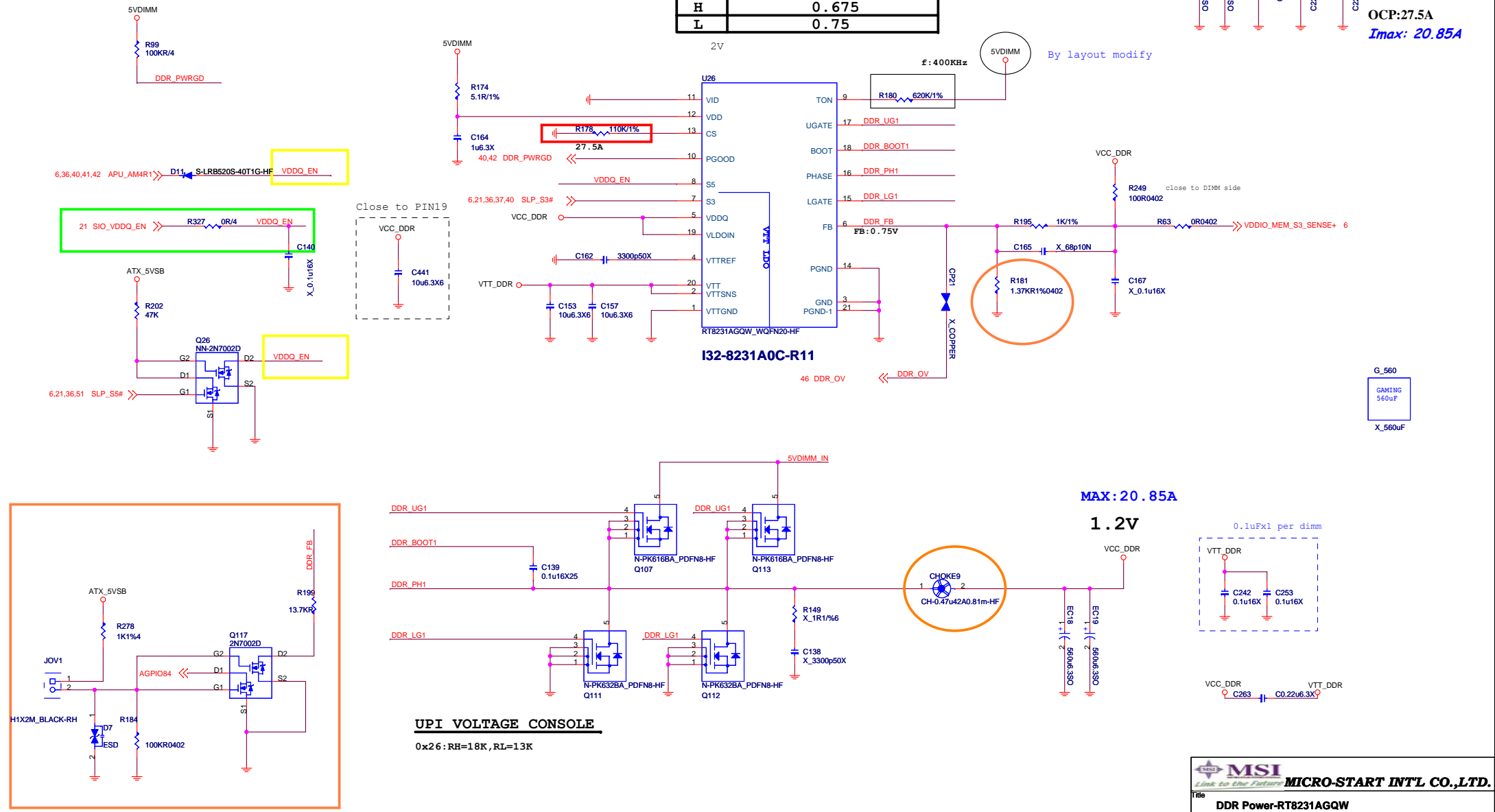


DDR4_1.2V 15.5A+4.75A+0.6A=20.85A
15.5A FOR CPU
4.75A FOR 2DIMM
0.3*2=0.6A FOR DDR VTT
OCP = 7.925A*1.5=11.8875A
Current limit= 110K(R178)*5uA/10/4mohm)=33A

$I_{rms} = I_{out} * \sqrt{D/N - (D)^2}$
 $VCCDDR:$
 $D = V_{out}/V_{in} = 1.2/5 = 0.24$
 $N = \text{Phase number} = 1$
 $= 20.85A * \sqrt{0.24 - 0.0576}$
 $= 5.21A$

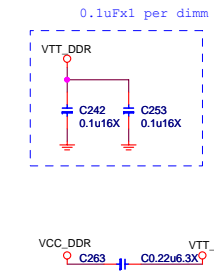
OCP:27.5A
I_{max}: 20.85A

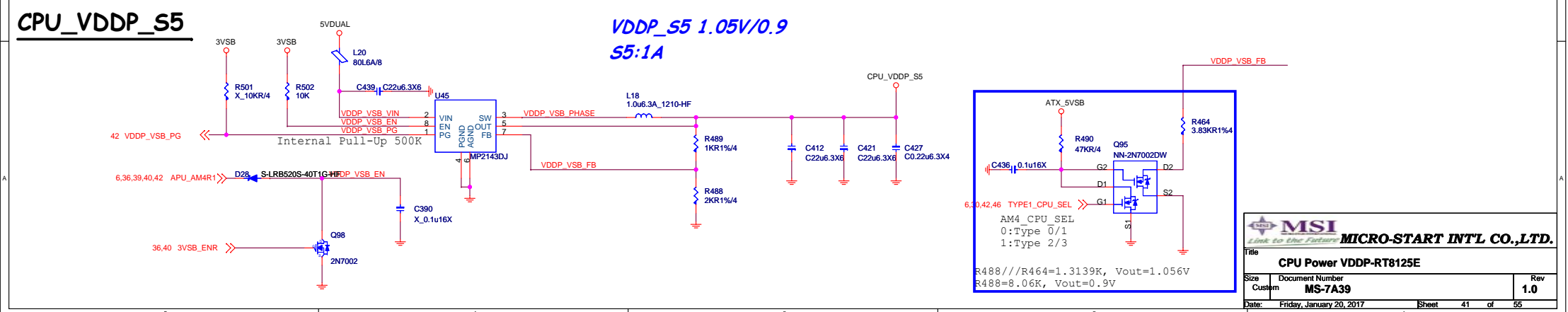
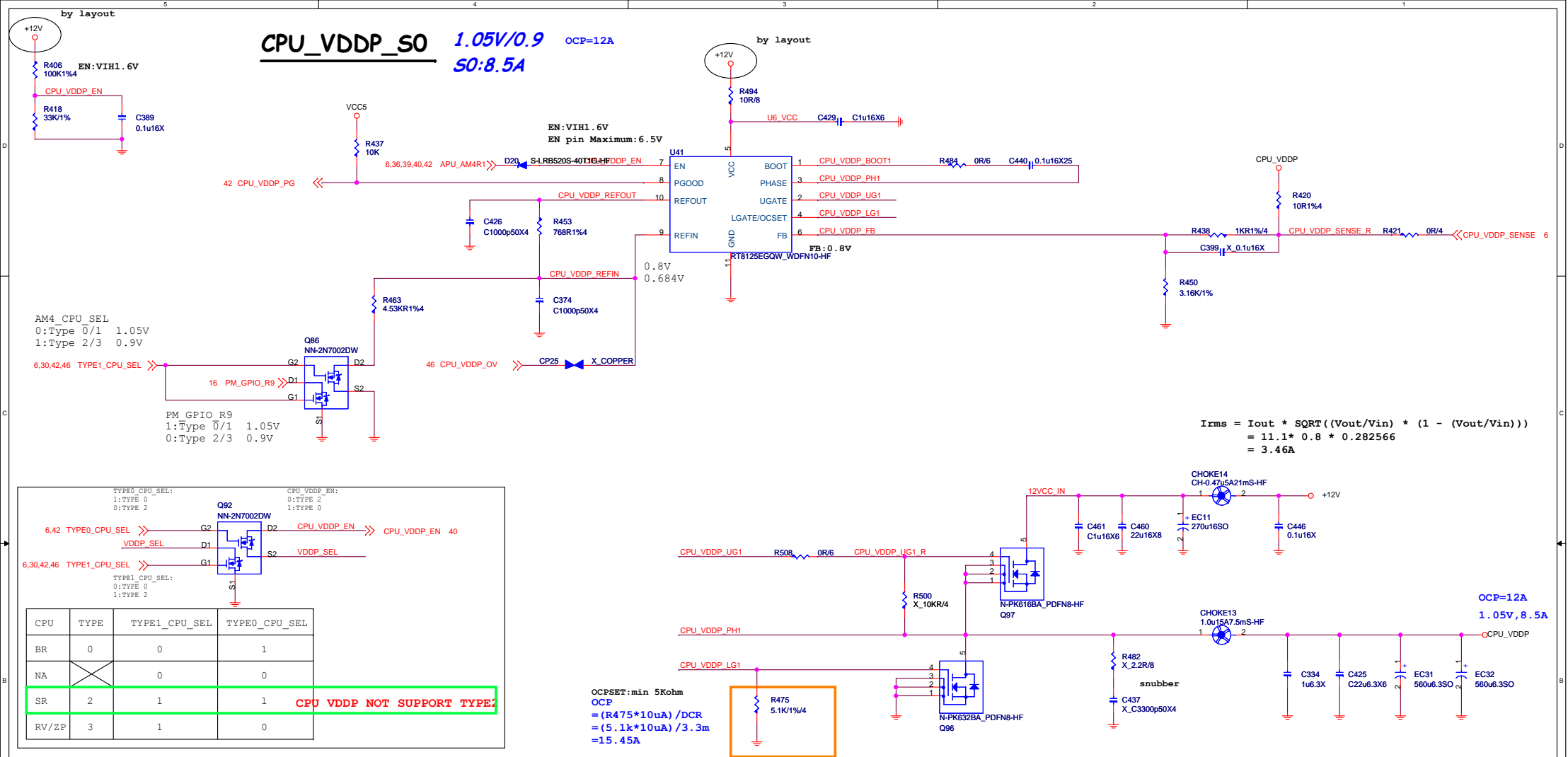
VID	Reference Voltage (V)
H	0.675
L	0.75



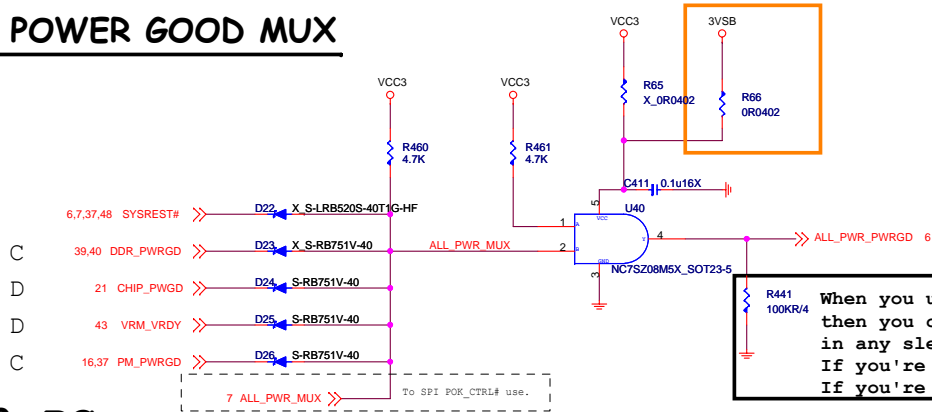
UPI VOLTAGE CONSOLE
 0x26: RH=18K, RL=13K

MAX: 20.85A
1.2V



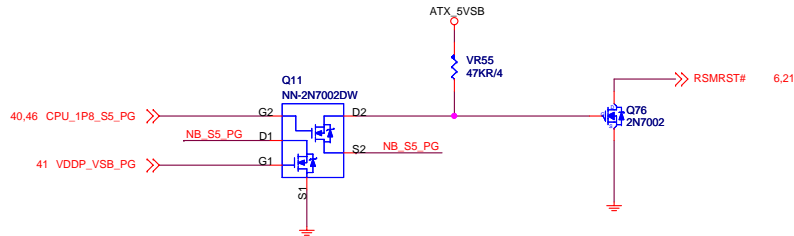


ALL POWER GOOD MUX

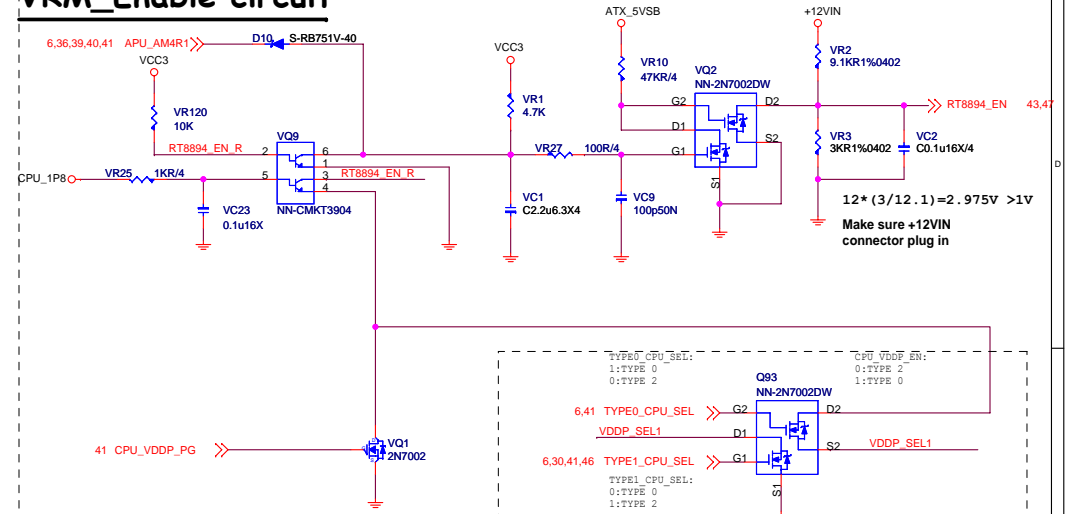


S0 PG

S5 PG



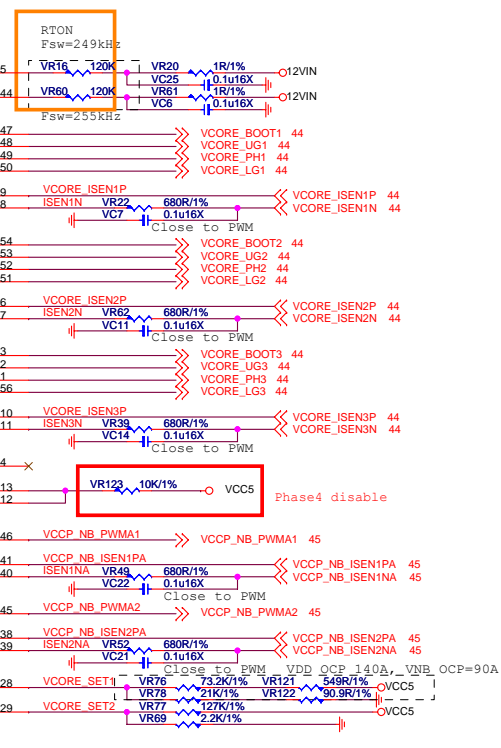
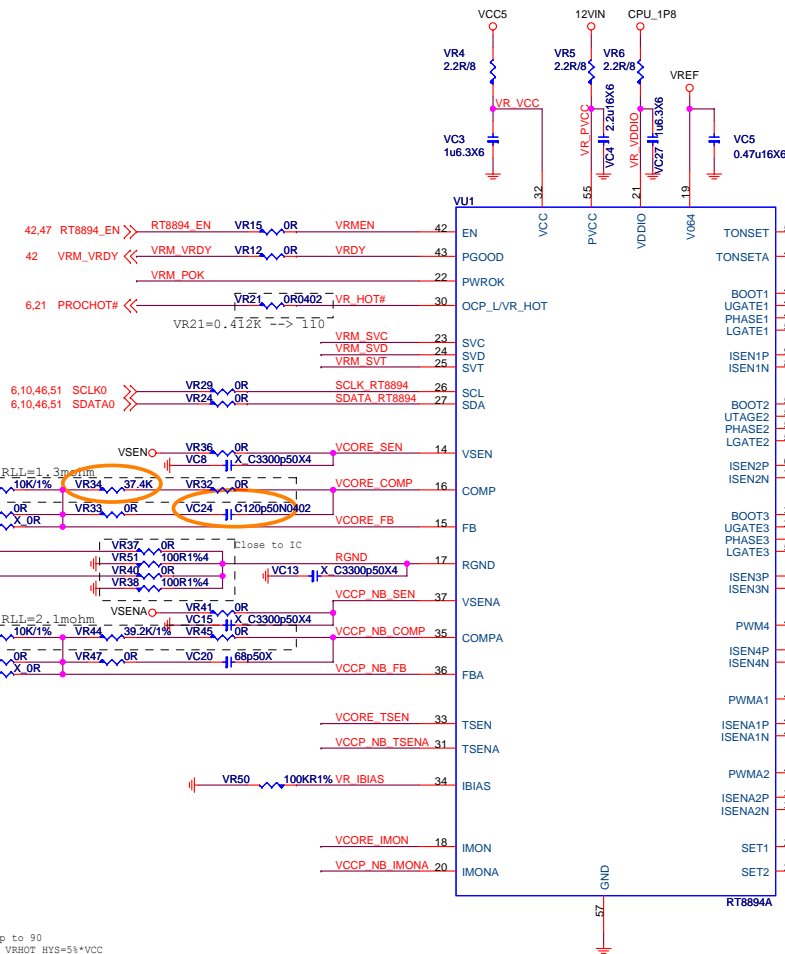
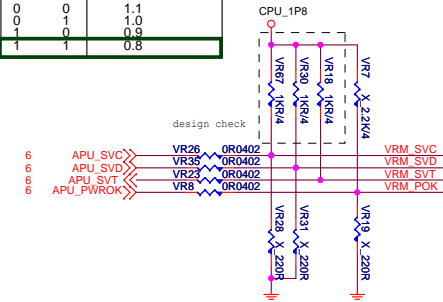
VRM_Enable circuit



CPU VDDP NOT SUPPORT TYPE2

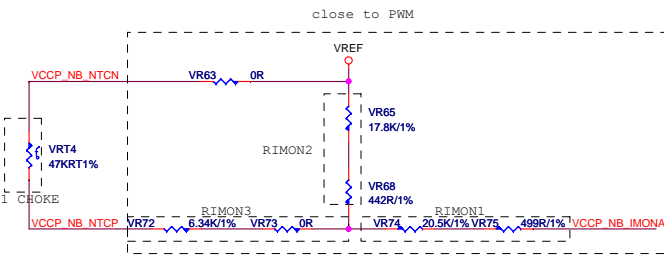
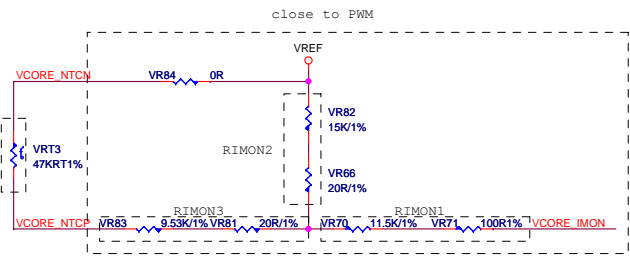
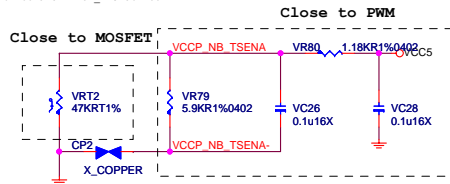
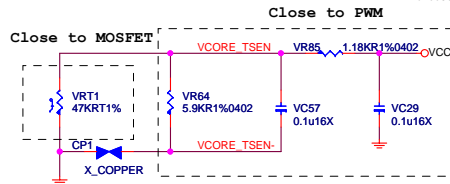
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

		BOOT VOLTAGE
SVC	SVD	Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

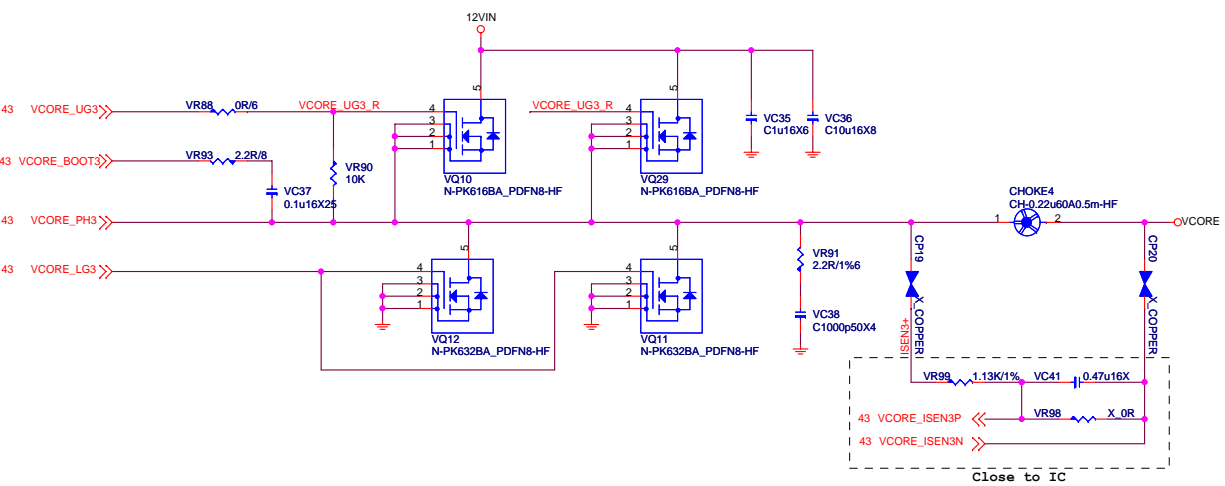
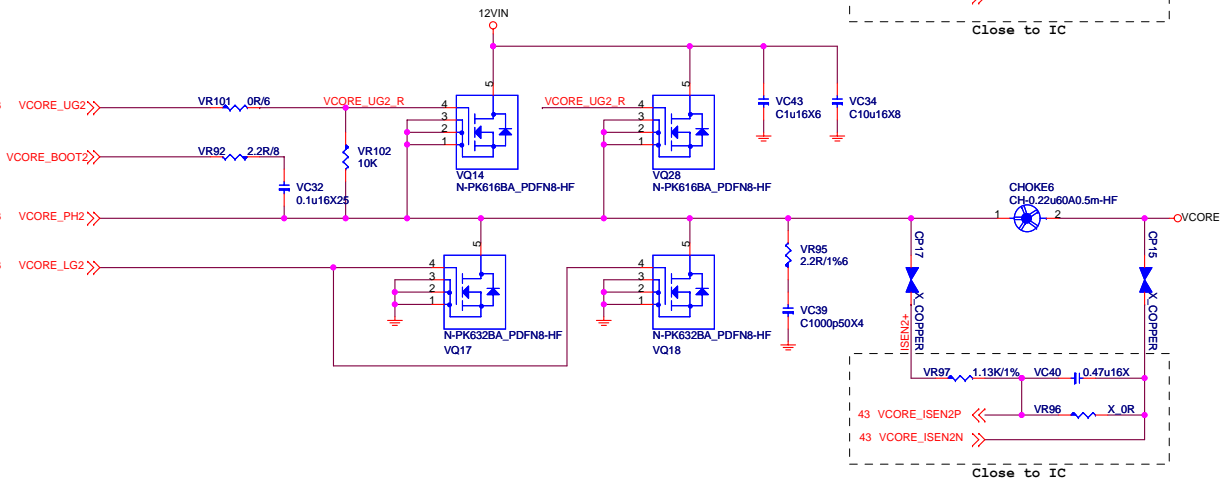
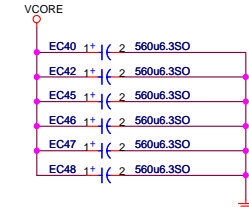
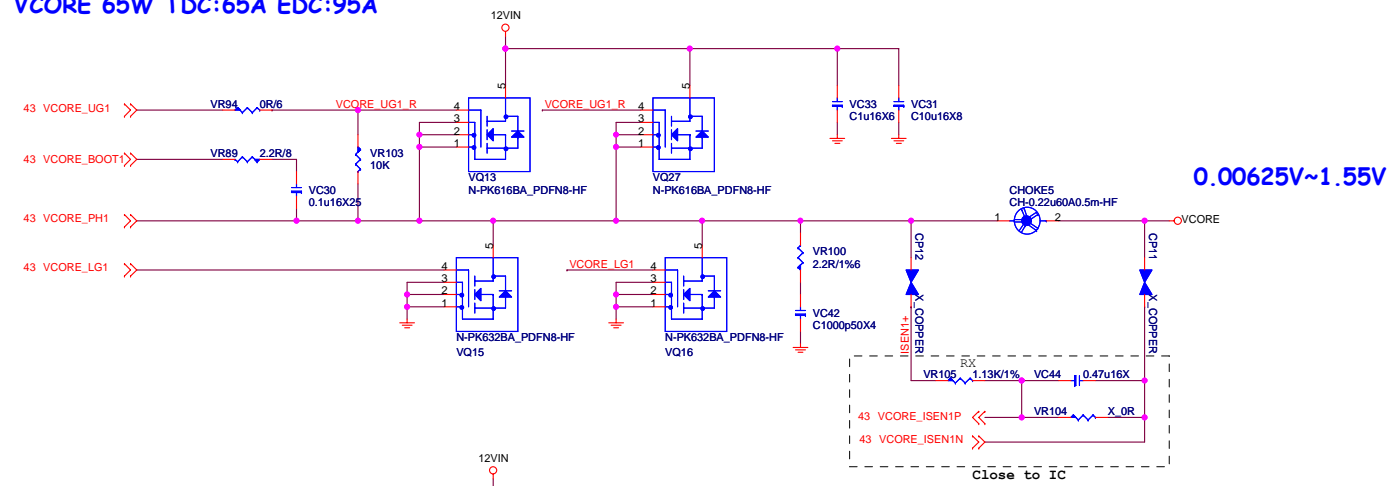


```
SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
```

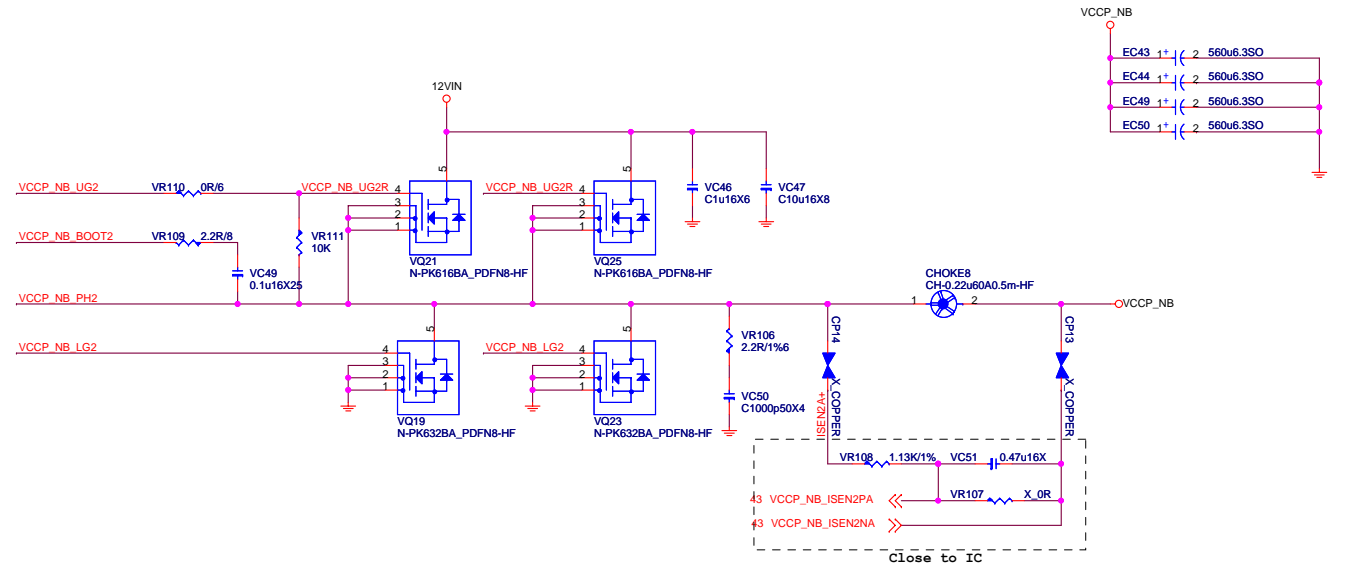
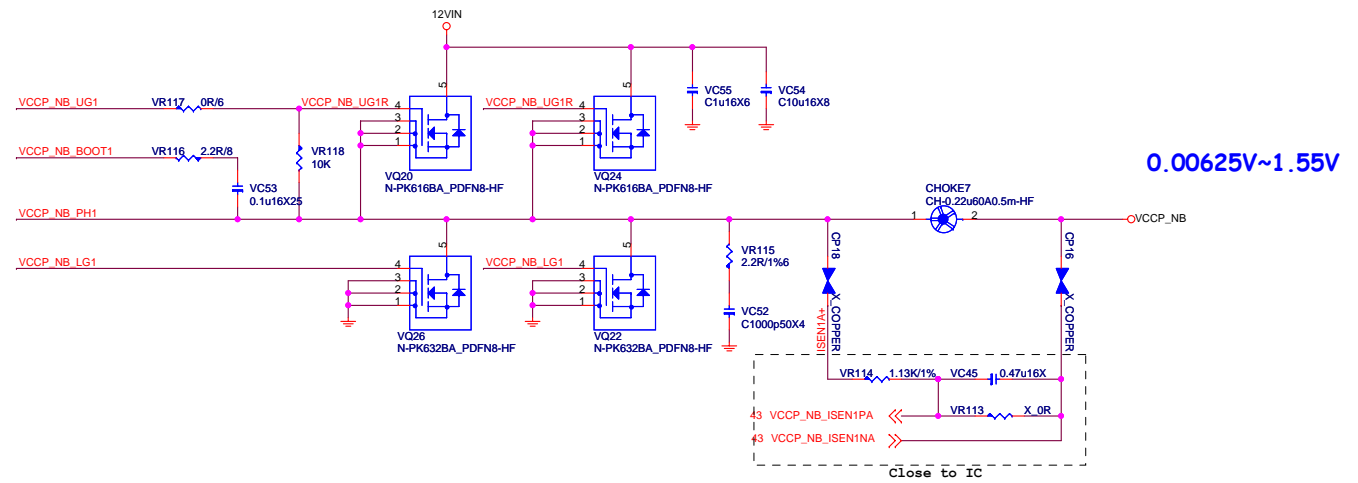
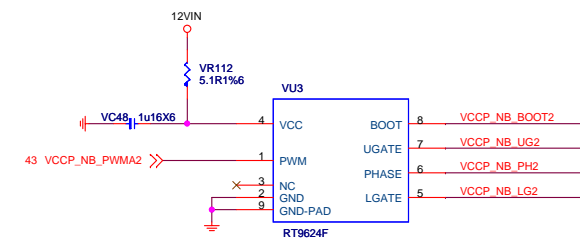
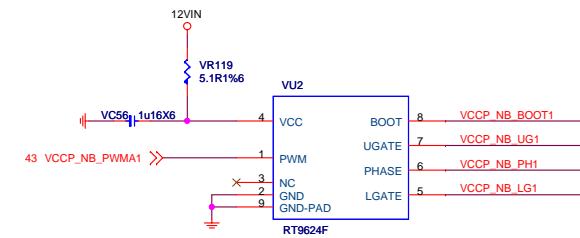
```
VCORE IccMAX: 125A =>OCP=>140A
VCC_NB IccMAX: 75A =>OCP=> 95A
```



VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A



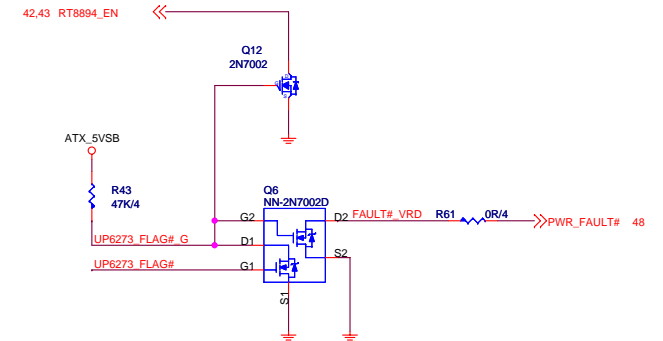
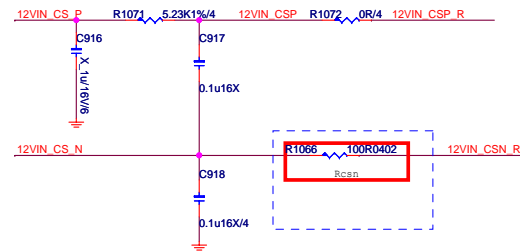
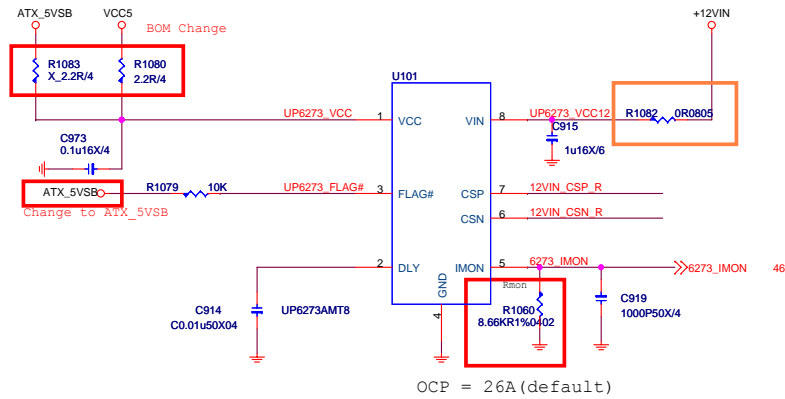
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A



uP6273 CURRENT SENSE

VCORE EDC MAC 125A

NB EDC MAX75A

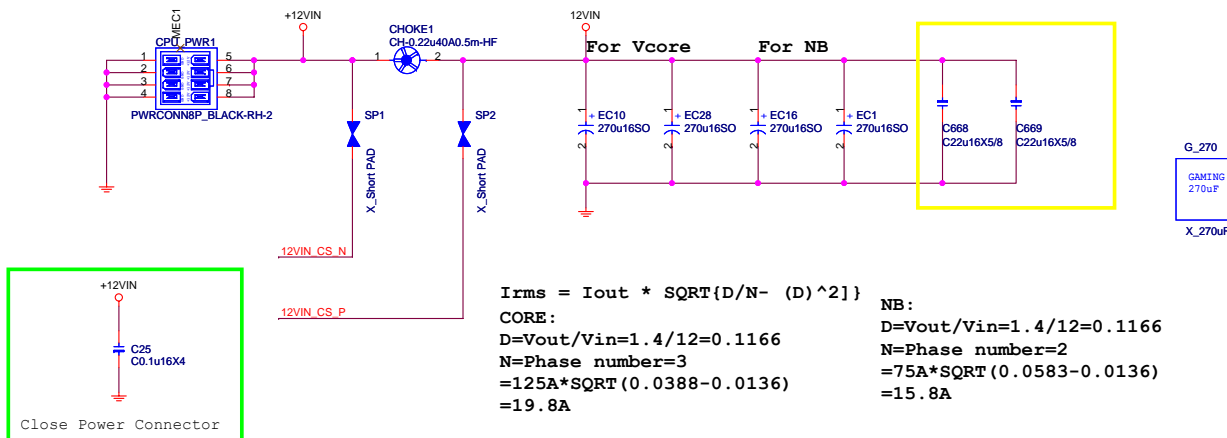


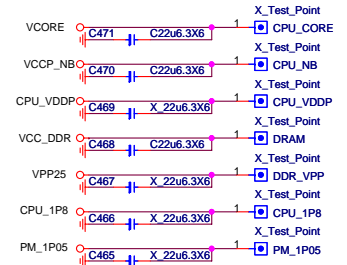
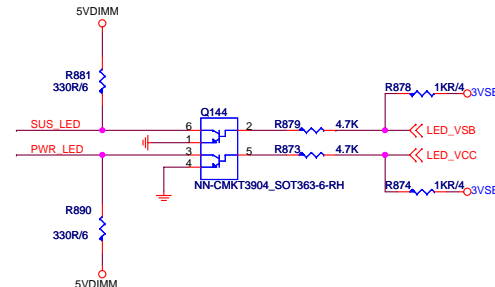
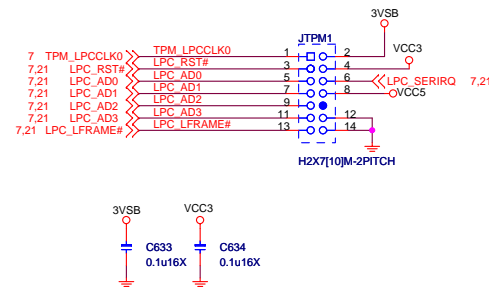
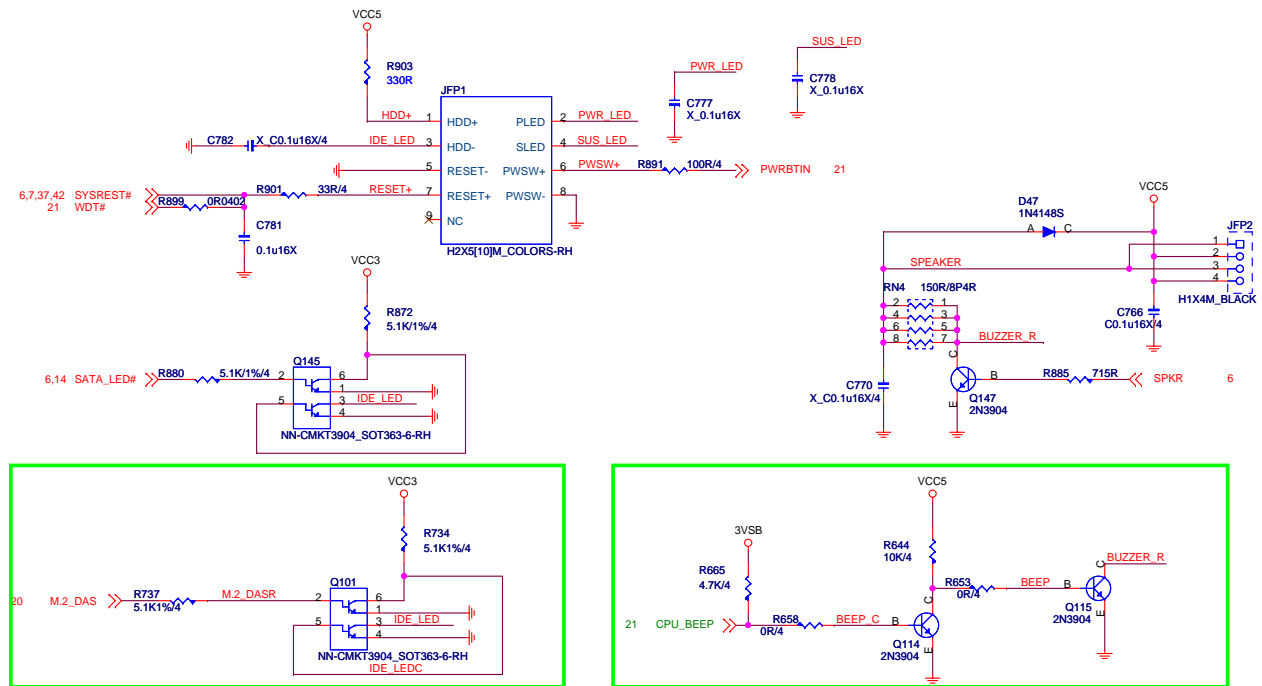
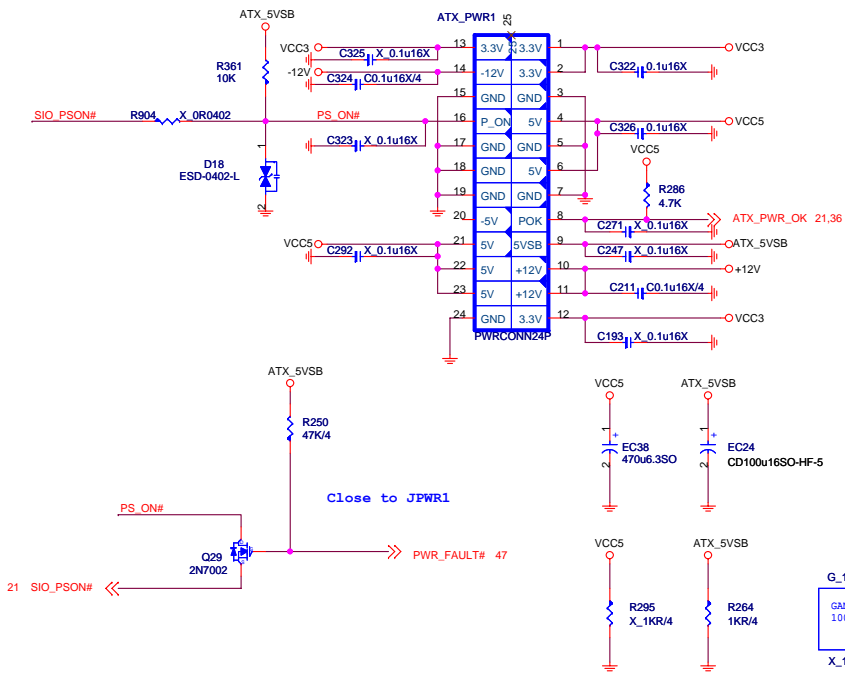
CPU POWER CONNECTOR

uP6273 CURRENT SENSE

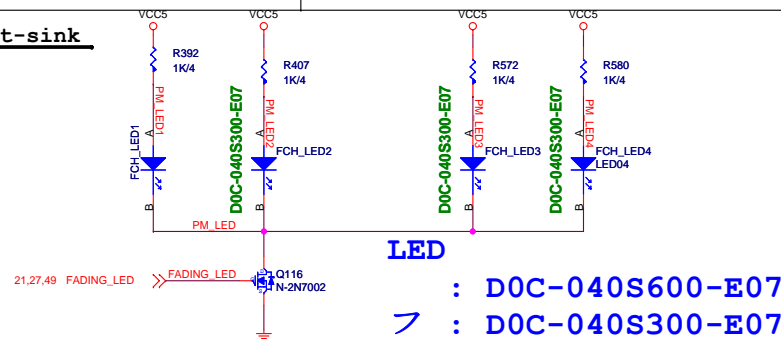
VCORE EDC MAC 125A

NB EDC MAX75A

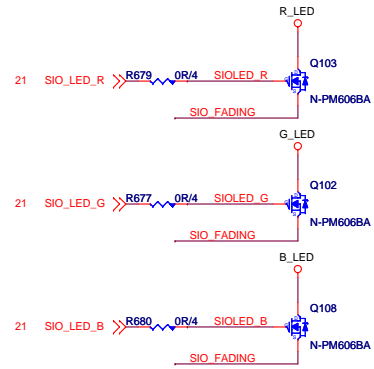




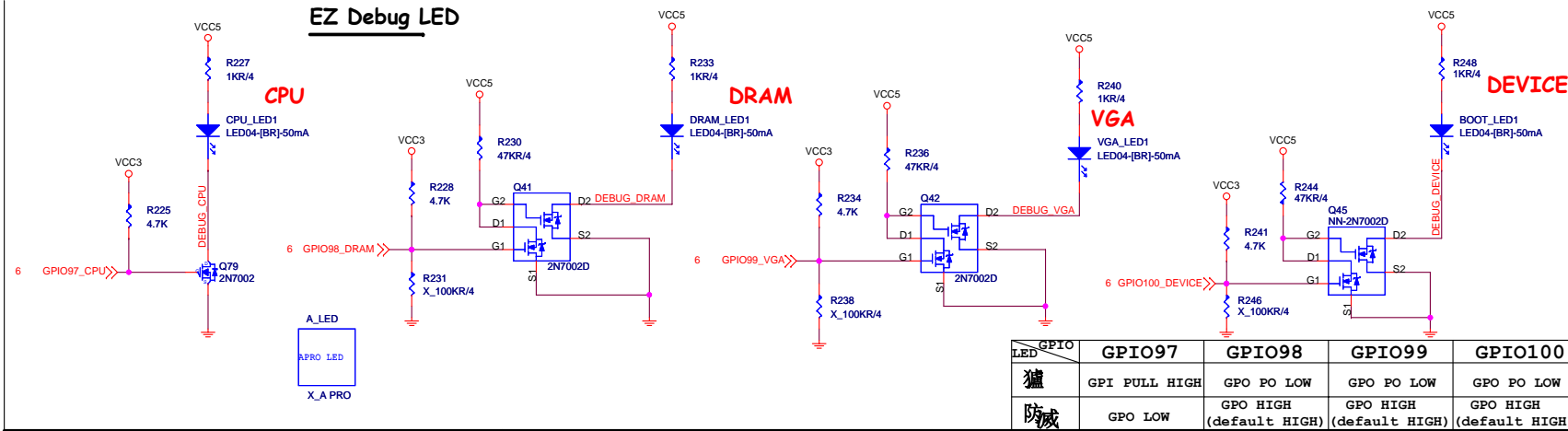
FCH LED Place under Heat-sink



LED Control by SIO

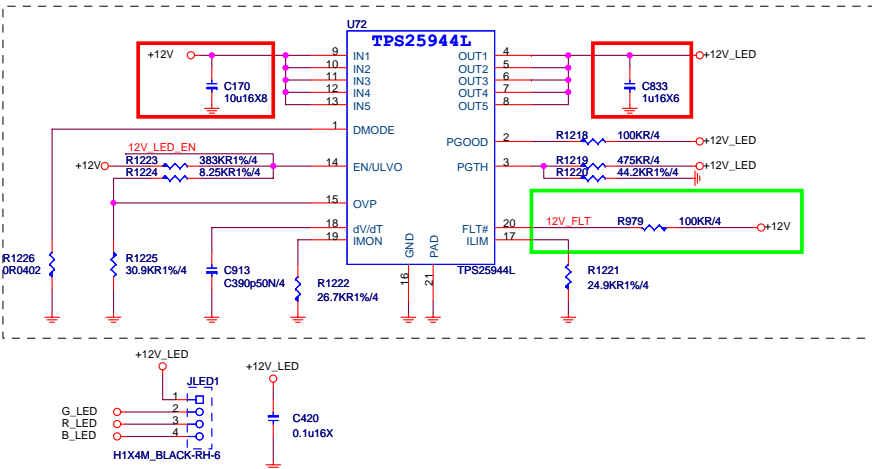


EZ Debug LED

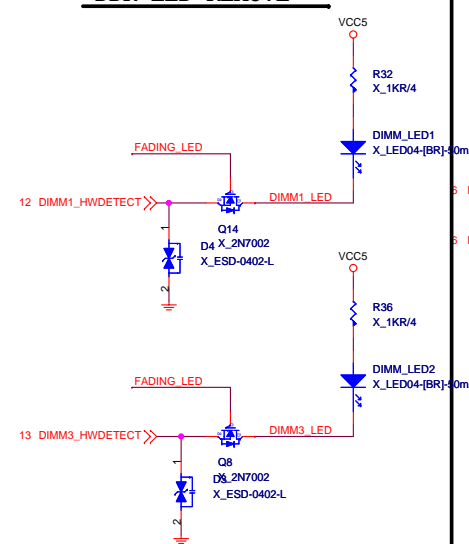


LED	GPIO	GPIO97	GPIO98	GPIO99	GPIO100
LED	GPIO	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
LED	GPIO	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

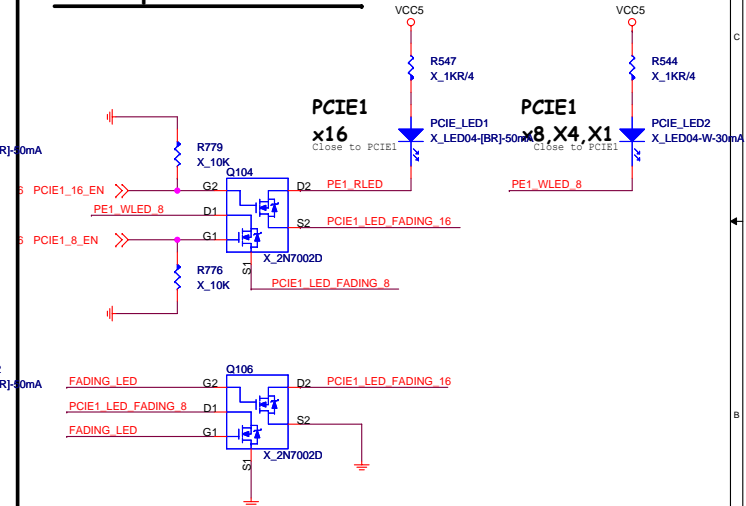
2016.07.06 Use TPS25944L



DDR LED REMOVE



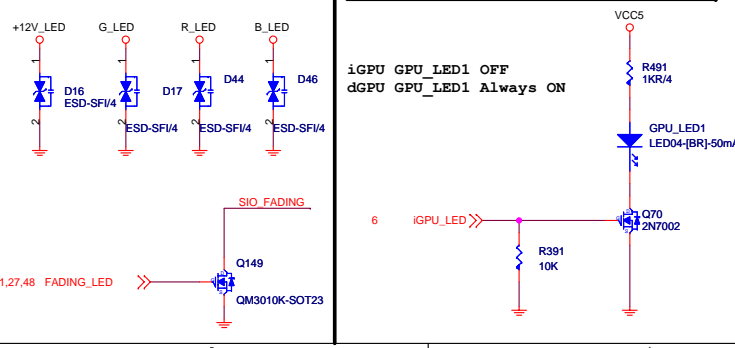
PCI Express LED Control remove



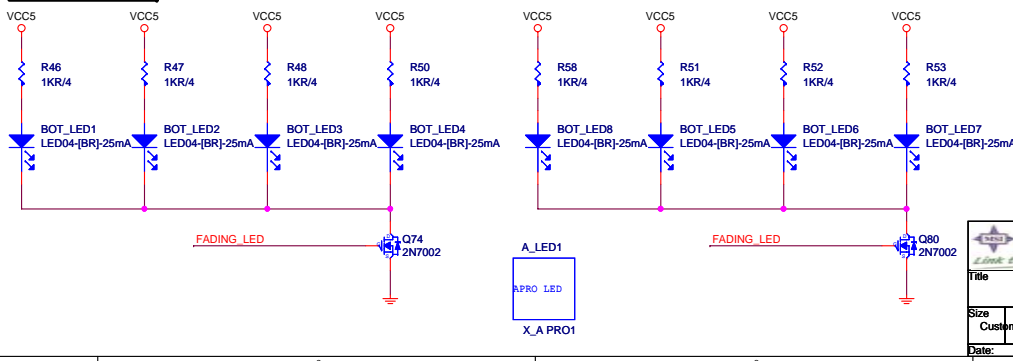
LED	x16	x8	x4
PCIE2	Red	White	White

GPIO	EGPIO95	EGPIO96
LED	GPI PO HIGH	GPI PO HIGH
LED	GPI (default LOW)	GPI (default LOW)

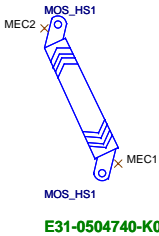
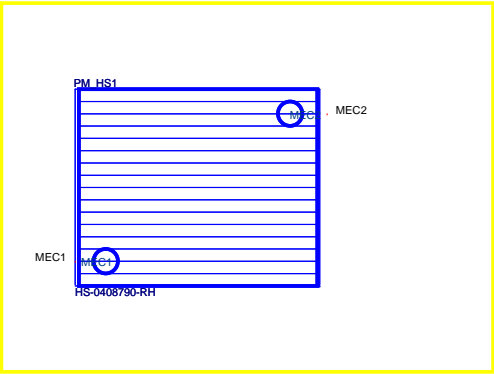
AM4 APU Detect LED Circuit



Bottom LED



HEAT SINK

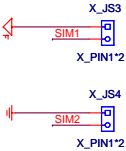


CPU Socket



RETENTION MODULE

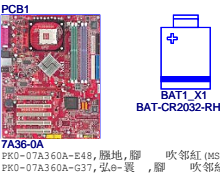
Simulation



MANUAL PART

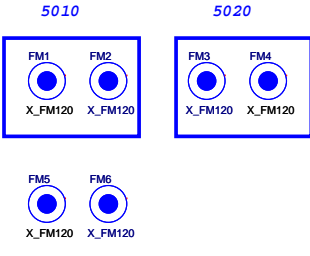
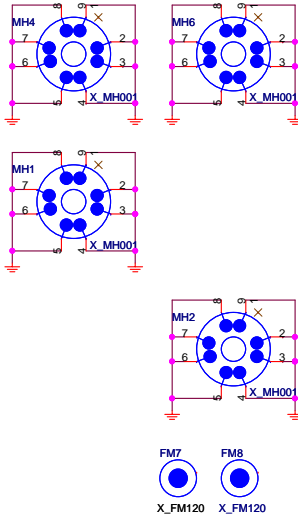
- HDMI_LA1
- Y01-RHDMI03-000
- SSE_LA1
- Y02-MA00101-SSE
- XSP_LA1
- Y02-MA00401-XSP
- CFOS_LA1
- Y02-MU00170-CFO
- MKT2
- G51-M1SPK3T-Q13
- MKT1
- G51-M1SPK3T-Q13

BIOS_LABEL




7A36-0A
P80-07A360A-E48, 腳 吹 鄰 紅 (MSIS)
P80-07A360A-G37, 弘 8- 實 , 腳 吹 鄰 紅 (MSIS)

Optics Orientation Holes



OPT	Configure	BOM	Function
		601-7A36-A01	XXXX

**MICRO-START INTL CO.,LTD.**

BOM OPTION

Size	Document Number	Rev
Custom	MS-7A39	1.0
Date: Friday, January 20, 2017		Sheet 50 of 55

